Logic analyzers and Xilinx ChipScope

1. About logic analyzers

For the examination of logic circuits and digital devices, one needs to register simultaneously plenty of digital (0-1) signals. The logic waveforms should be stored for evaluation. This can be done with a logic analyzer. The schematic of a logic analyzer is shown below.



The signals of the device under test (DUT) are connected to D1..N analyzer inputs. The POD performs signal conditioning towards the stable detection of the logic levels. The signals will be sampled and stored in the state memory. The sampling is scheduled by the SCK Clock. The analyzer has two different modes:

In **state analysis mode** the sampling clock is the same as the DUT clock (connected to the ECK input of the analyzer), the sampling itself is synchronous. The DUT states will be stored in the state memory.

In **timing analysis mode** the analyzer uses its own internal clock source (ICK) for sampling, the timing of the DUT can be evaluated, if the ICK frequency is high enough. This frequency must be selected carefully, determined by the desired resolution in time and the relevant input signal length. (A high frequency ICK results high accuracy but the state memory will be filled rapidly.)

The sampling is controlled through the **trigger condition**. After the condition is fulfilled, the sampling is stopped and the state memory can be read (displayed). The exact trigger position can be set up, pre- and post-trigger events can be evaluated.



2. The Xilinx ChipScope

The ChipScope is a logic analyzer implemented in the FPGA together with the designed hardware to test (DUT). Both DUT and ChipScope use the System Clock, thus ChipScope is used generally for state analysis.

The ChipScope can be added to a design and configured with ChipScope Core Inserter. ChipScope Analyzer is the GUI for the measurement

2.1. Using ChipScope Core Inserter

Add a ChipScope Definition and Connection File as a new source to your project!

Select Source Type Select source type, file name and its location. BMM File ChipScope Definition and Connection File Implementation Constraints File IP (CORE Generator & Architecture Wizard) MEM File Schematic User Document Verilog Module Verilog Test Fixture VHDL Module VHDL Module VHDL Library VHDL Package VHDL Test Bench	Eile name: cs_cntr Logation: C:_Projects\BME\Education\ml1_2011_2012\ISE
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Double clicking the cdc file, you can open the core inserter. In the first window just click next!

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The Integrated controller (ICON) is the main modul interfacing the PC through the JTAG cable and the Integrated Logic Analyzer (ILA) moduls. Using a Spartan-3 FPGA, ICON has no configuration parameters and only one ICON module can be used, so click next!

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16 ILAs can be connected to one ICON, but during the lab exercises you will need only one. The ILA configuration defines the parameters of the logic analyzer. In the main window, you can see the currently used resorces (LUT,FF,BRAM count) and the configuration options on the right side.

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Trigger parameters

You can define maximum 16 trigger ports. Each of them can use different trigger signals. The trigger conditions can be defined by means of Match units. The match units can count the fulfilled trigger conditions, so it is possible to trigger for example on the 42th rising edge of a signal. First and last, the **number of trigger ports** must be given, and you have to define **the trigger bitwidth**, **number of match units** and **counter width**. The **match type** must be one of the following:

- Basic: the trigger condition can be defined with 0,1 or X (don't) care bit values.
- Basic w/edges: besides the signal levels, edges can be specified in the trigger: <u>R</u>ising edge, <u>Falling edge</u>, <u>Both edges or No transition</u>.
- Extended: bit values (0,1,X) and trigger world relations (equal, less/greater than...) can be evaluated.
- Extended w/edges: same as previous and edges (R,F,B,N)
- Range: extended and range check (Check if trigger word is between two defined values)
- Range w/edges: same as previous and edges (R,F,B,N)

Trigger sequencer makes it possible to trigger only if various match unit conditions are met in the defined order. **Sequencer level** must also be defined. E.g. $M0 \rightarrow M1 \rightarrow M0$ is a 3 level sequence (using 2 match units.)

If **enable storage qualification** is checked, the sampling (based on system clock edge) can be enabled/disabled by means of a match unit.

Capture parameters

You can select, whether the data bits to sample are the same as the trigger port bits (**Data same as trigger**). The sampling occurs on rising or falling edge of the system clock. **Data depth** gives the size of the state memory in words. (The word length is the bit-width of the data port.)

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The connections between the DUT and ChipScope can be defined after clicking on 'Modify connections'. The *post-synthesis signals* of the DUT can be assigned to ChipScope channels.

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Generally, in a proper design register names will be kept after synthesis, but combinational logics can be simplified. The base type gives the module type of the signal source:

- BUFGP: clock buffer. Use this as the ChipScope clock signal
- IBUF: input buffer, connected to an FPGA pin, used as input.
- OBUF: output buffer, connected to an FPGA pin, used as output.
- IOBUF: bi-directional buffer. It cannot be connected to ChipScope.
- GND/VCC: constant logical 0/1.
- FD*: some version of D flip-flop (eg.: FDRSE is a D FF with reset, set, enable).
- LUTx stands for Look Up Table with x used inputs.

The patter field can help to search for the desired signals. You can use wildcards. After assigning all ChipScope channels you can return to project navigator.

DETRUC	ILA	Select Integrated Logic Analyzer Option
E KON	Trigger Parameters Capture Parameters Net Connections	
OC.ILN	Net Connections	
	CLOCK PORT CH0: /dk_BUFGP TRIGGER PORTS	
LUT Count 469 SF Count 425 BRAM Count 1	• TRIGO CH9: //seg7/dk_div=0+ CH1: //seg7/dk_div=1+ CH2: //seg7/dk_div=1+ CH2: //seg7/dk_div=2+ CH4: //seg7/dk_div=3+ CH4: //seg7/dk_div=3+	
	Modify Connections	
	< Previous Return to Project Nevigator	Remove Un
ssages ading CDC project D (BME)Edu	cation/4LAPLAB_VILL1_20112012cs_projiChipscopeics_1.cdc	

The design with the CDC file must be re-synthesized. The synthesis of the analyzer takes quite long time, and it must be repeated every time when you change the chip scope configuration. So double-check the settings if you want to analyze a design!

2.2. Analyzis with ChipScope

Download the new bit-file and start the ChipScope Analyzer GUI! Select JTAG Chain/Xilinx Platform USB Cable in the upper menu, click Ok on the pop-up windows to connect to ChipScope module!



Select File/Import to import the signal names and define busses based on the cdc file you have made before!

Signal Import	
Import File	
File	cs_1.cdc
Directory	D'BME/Education/ALAPLAB_VILL1_20112012/cs_proj/Chipscope/
	Select New File
UnitiDevice	
	DEV: 0 UNIT: 0 (ILA)
	Clinite controllings
	V and Grate Bases
	OK Cancel

In our example, the signals are the 12-bit clock divider and the 4-bit anode signal for a 4-digit 7-segment display controller.

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New Project	1 Incant Senat-D	VO NO	0.00005250ELUMPTION	NCADILAL			10
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	D)						
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All the match units are initially set to don't care.

Trigger setup

For the **match units**, you can set up a trigger conditions. The possible settings depend on the match unit type. *Don't care bits are only allowed, if the function is equal* (==) *or not equal* (<>), in all other cases, all bits of a match unit must be defined!

Add	Active	< (#	24	er Condition Name Trigge	er Condition Equa	don	
- Lond Hilds I -		>=					
· CTM3 Tr	iogerPart1			10000	Bin	disabled	
- M2:Tr	iggerPort0	0		3000(J000(J000)	Bin	disabled.	
- 🗂 M1:Tr	iggerPort0			2020(_)000(_)000(Bin	disabled	
← ☐ M0:Tr	ggerPort0	=		3000(_2000(_2000)	Bin	diundied	-
	atch Unit	Function		Value	Radix	Counter	

The **trigger condition** can be defined as a logical function or a sequence of match unit conditions. Click on 'Trigger condition equation' to set it!

2	Add	Active	Tripper Condition Name	Lucter Condition Equation	
6u	Der		TriggerCondition0	MO	*

The sampling can be set up using the **capture** panel. In window mode you define, how many trigger conditions should be stored in the state memory during the session. In N samples mode, the number of words to stored after one trigger is defined. Setting the (trigger) position to grater than 0, the samples before the trigger event can be examined.



You can assign the logical combination of match units not only to a trigger condition, but also to a storage qualification enable signal. E.g. you can configure the ChipScope to sample the data only if M3 match unit condition is fulfilled.

Chicke a no channi C or channi		171 Median Autora Editorio		
Match Unit	Enable	Tregate		
			-1	
142				
102	2			
orage Condition Equation				
	M3			

<u>Analysis</u>

After the apropriate setup, the analysis itself can be started using the **toolbar of the ChipScope**. In 'Single' trigger run mode after pressing the 'Play' button, the analyzer waits for trigger, after the trigger it fills the state memory and if it is full, the result can be

examined in the **waveform window**. You can stop the analyzer any time, but the waveform is refreshed only if the the state memory is totally filled. (Thus, for "sorter" waveforms set depth in capture panel!)



Using the "T!" button, sampling can be started immediately (the trigger condition is not considered.). Selecting the 'Repetitive' trigger run mode, the analyzer waits automatically for the next trigger event after the state memory is fulfilled.

Reference

The detailed documentation of the ChipScope can be downloaded from the Xilinx webpage. http://www.xilinx.com/support/documentation/dt_chipscopepro_chipscope13-2.htm