Exercise 9.

Basic Logic Circuits

(Revised by Tamás István Krébesz - MIT on 28/08/2018)

Required knowledge

- Measurement of static characteristics of nonlinear circuits.

- Measurement of current consumption.

- Measurement of dynamic properties of electrical circuits.

- Definitions related to logic circuits.

Aim of the measurement

- Measurement of typical properties and features of logic circuits using TTL and CMOS inverters.

- Measurement of static properties like voltage transfer characteristic, load dependence of output voltage levels, etc.

- Dynamic characteristic like delays, rise time, fall time, etc.

- Comparison of measurement data against data sheet data.

- Measurements of Flip-flop properties (truth table, setup and hold time).

Keywords

basic logic circuits, TTL, CMOS, voltage transfer characteristic, voltage levels, delays, rise time, fall time, setup time, hold time.

Introduction

Basic logic functions like AND, OR, XOR can be realized in many ways. In the first electronic devices relays and vacuum tubes were used for this purposes. In 1947 the transistor was invented at Bell Laboratories. This resulted in solid state switching, that is much faster and more reliable than relays. Therefore this enabled the creation of complex logic functions in small chips. In 1958 the first integrated circuits were invented.

One of the simplest integrated ICs are the basic logic circuits. Many logic gate types are produced as individual components, each of them contains one or more basic logical functions, which could be used as building-blocks to create systems or to interconnect complex integrated circuits. There are many types of logic circuit families depending on their properties and technologies (RTL, DCTL, TTL, CMOS, ECL etc.).

Laboratory exercises 1.

The aim of this laboratory is to introduce the typical properties and features of two widespread logic families the TTL (Transistor-Transistor Logic), and the CMOS (Complementary Metal–Oxide–Semiconductor logic).

Although the use of the TTL family is reduced in the past years, the fundamental terms like rise-time, transfer characteristics, and their dependencies on environmental conditions can be learned easily by measuring these devices. The logic gate ICs used in the measurements are non ideal ones, which can cause problems in real systems. The measurements will show examples of these non ideal features of logic gates. The terms learned here can also be used in the applications of complex devices like microcontrollers or FPGAs (Field Programmable Gate Array).

Fundamental terms

The data sheet of an integrated circuit contains many information, for example:

- operating conditions (timing, worst case values, static electrical characteristics etc.)
- absolute maximum ratings (over these limits the ICs is subject to damage)
- packaging and mechanical information (pin outs, and packet dimensions)

The properties above are vital for using the ICs appropriately, therefore we have to understand the meaning of the most important terms.

Logic voltage levels

In digital circuits, the binary logic levels of 0 (Low) and 1 (High) are represented by the voltage difference range between the signal and ground. The range of voltage levels that represents the binary level of 0 or 1 depends on the logic family being used. The range tolerances of voltage levels are dependent on whether they are representing an input or an output. The tolerances are stricter for output voltage levels comparing to the input levels (Figure 9-1.), due to the noises that can affect the signal on the rute between the outputs and the inputs. The data sheets usually provides the worst case values of logic voltage levels like U_{Hmin} and U_{Lmax}. For example the traditional TTL logic family has the following voltage levels $U_{Hmin} = 2.0$ V, $U_{Lmax} = 0.8$ V for the inputs, and $U_{Hmin} = 2.4$ V, $U_{Lmax} = 0.4$ V for the outputs. The 5 V CMOS logic families usually have the following logic voltage levels: $U_{Hmin} = 3.85$ V, $U_{Lmax} = 1.35$ V for inputs, and $U_{Hmin} = 4.9$ V, $U_{Lmax} = 0.1$ V for outputs.
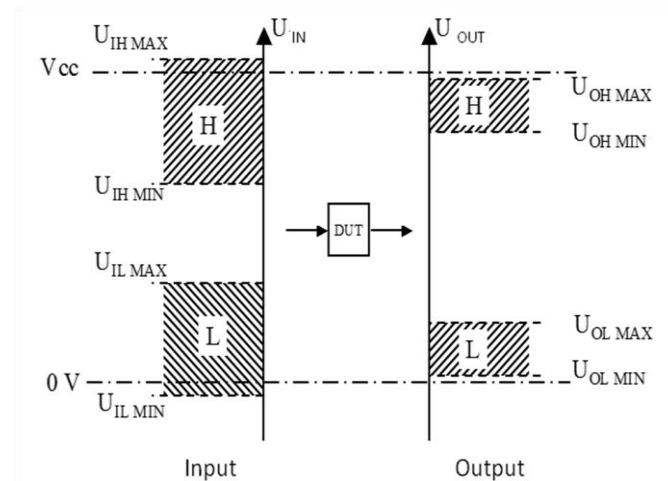

Figure 9–1.: Logic voltage levels

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Transfer characteristic

Voltage transfer characteristic represents how the output voltage changes depend on the input voltage. If there are more than one inputs in the system, then the voltage transfer characteristic can be specified and measured for every inputs individually. In this case the non-used-inputs should be held in a static Low or High state.

Rise time, Fall time, delays

Rise time: the time interval for an output waveform to rise from 10% to 90% of its total amplitude (Figure 9–2.).

Fall time: time interval for an output waveform to fall from 90% to 10% of its total amplitude (Figure 9–2.).

Switching point: The point of the characteristic where the input voltage equals to the output voltage is called switching point. The logic gates interpret the voltage levels below the switching point as logic Low or 0, above the switching point as logic High or 1.

Delay, gate delay: The time interval between the change of the input signal and the change of the output signal (it tells us how much time is needed for the output signal to be changed when the input has already been changed). The gate delay is ideally measured between the switching point of the input and the output. This point for the SN74, SN74S, SN74F family of ICs is 1.5 V, for the SN74LS, SN74 AS, SN74ALS family of ICs the switching point is 1.3 V. The switching points of the CMOS ICs are usually hard to specify therefore U_{Hmin} or U_{Lmax} is used instead.

In practice the gate delay measurement is made between the 50% level of the input waveform to the 50% level of the output waveform. There are differences between the High to Low and Low to High gate delay times, therefore both of them should be measured (Figure 9–3).
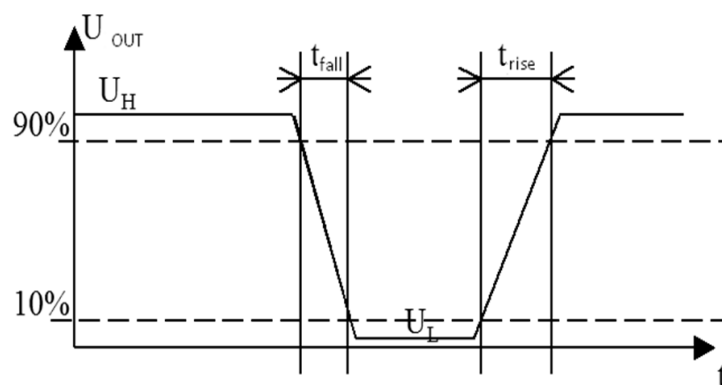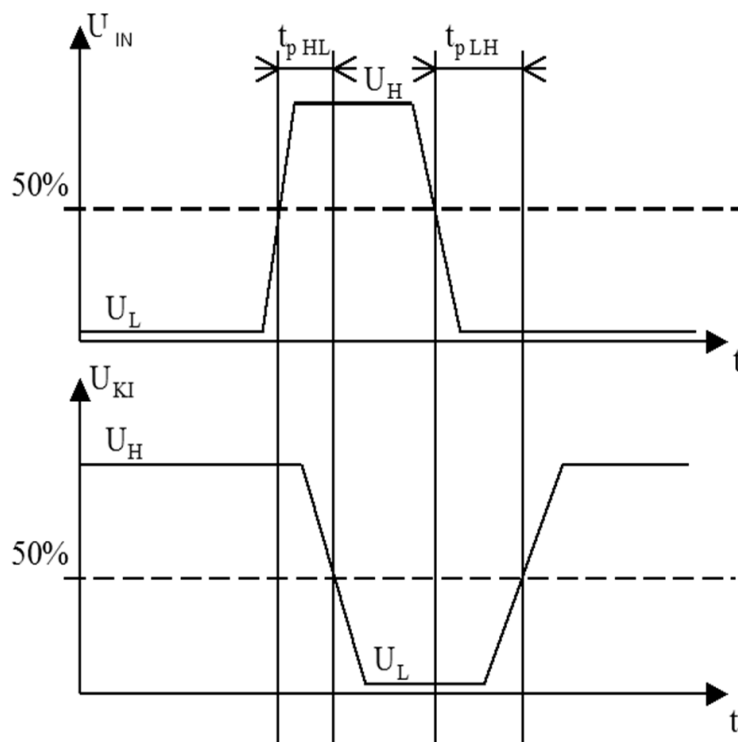

Figure 9–2.: Fall and Rise time

Laboratory exercises 1.

Figure 9–3.: Gate delay

Load driving ability (FAN OUT)

Load driving ability of a digital output is the highest current value when the output is still able to work in the guaranteed voltage level ranges. For logic gates the load driving ability is usually specified as fan-outs. The maximum fan-out of an an output is the greatest number of inputs of gates of the same type to which the output can be safely connected. In other words, the fan-out tells us how many input gates can be connected to the output.

Setup time, hold time, propagation delay for Flip-Flops

Setup time: is the minimum amount of time the synchronous data signal line should be held steady before the clock event. The setup time is used to ensure the reliable sampling of the data.

Hold time: is the minimum amount of time the synchronous data signal should be held steady after the clock event. The hold time is used to ensure the reliable sampling of the data.

Propagation delay: is the time a flip-flop needs to change its output after the sampling clock edge. There are differences between the High to Low and Low to High propagation delays.

Temperature dependency

Logical circuit's operation parameters are temperature depended. In the case of TTL ICs the base to emitter voltage of transistors are depend on temperature, therefore the output high level and the switching point are also temperature dependent (in a few mV/ ºC range). The temperature dependency of the propagation time in not too significant, maximum 10% in the normal operation range. In the case of CMOS ICs the switching point is not really temperature dependent, but their propagation delay has about a 0.3%/ºC temperature dependency, therefore at high temperatures the propagation time of a CMOS IC can be 20% to 30% higher than at room temperature.

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There are operational temperature range classes for integrated ICs. Usually a semiconductor is assigned to one of the following classes (based on AEC-Q100 standard):

- grade 4 (commerce):   0 ... +70 ºC,
- grade 3 (industrial):   -40 ... +85 ºC,
- grade 2:   -40 ... +105 ºC.
- grade 1:   -40 ... +125 ºC.
- grade 0:   -50 ... +150 ºC.

The TTL circuit family

TTL (transistor-transistor logic) uses bipolar transistors to form its integrated circuits. The first TTL family of integrated circuits was produced by Texas Instruments in 1964, that was the SN54 and SN74 series. The SN54 family has a higher temperature range, and it is intended primary for military and extended industrial use. Over the years many TTL variants and versions were developed to improve speed, reduce power consumption, or both.

The SN74L series is slower than the original SN74 (typical delay of SN74L series is about 30ns, where the SN74 series has about 10ns delay), but it has a less power consumption (SN74 has about 1mW/gate power consumption while SN74 series has about 10mW). The first Schottky technology based TTL IC was introduced in 1969. The normal Schottky SN74S series have less delay (to about 3ns), but raised the power consumption (to about 20mW). The Low-power Schottky series SN74LS were introduced in 1971 and it has a very low power consumption: about 2mW/gate, and a fair delay (about 10ns). Among the last TTL families in 1980s the TTL-F (Fast), TTL-AL (Advanced Schottky) TTL-ALS (Advanced Low-power Schottky) series were also introduced with improved speed and/or with reduced power consumption.

Fundamental TTL gate circuit

The fundamental TTL circuit is a TTL NAND gate (Figure 9-4.). The TTL inputs are the emitters of a multiple-emitter transistor (T1) followed by a common emitter amplifier (T2). The output of the NAND gate is a "totem-pole" push–pull style output (T3, T4). The D1, D2 diodes have a protection role to cut off the negative pulses from reflections or other noise sources.
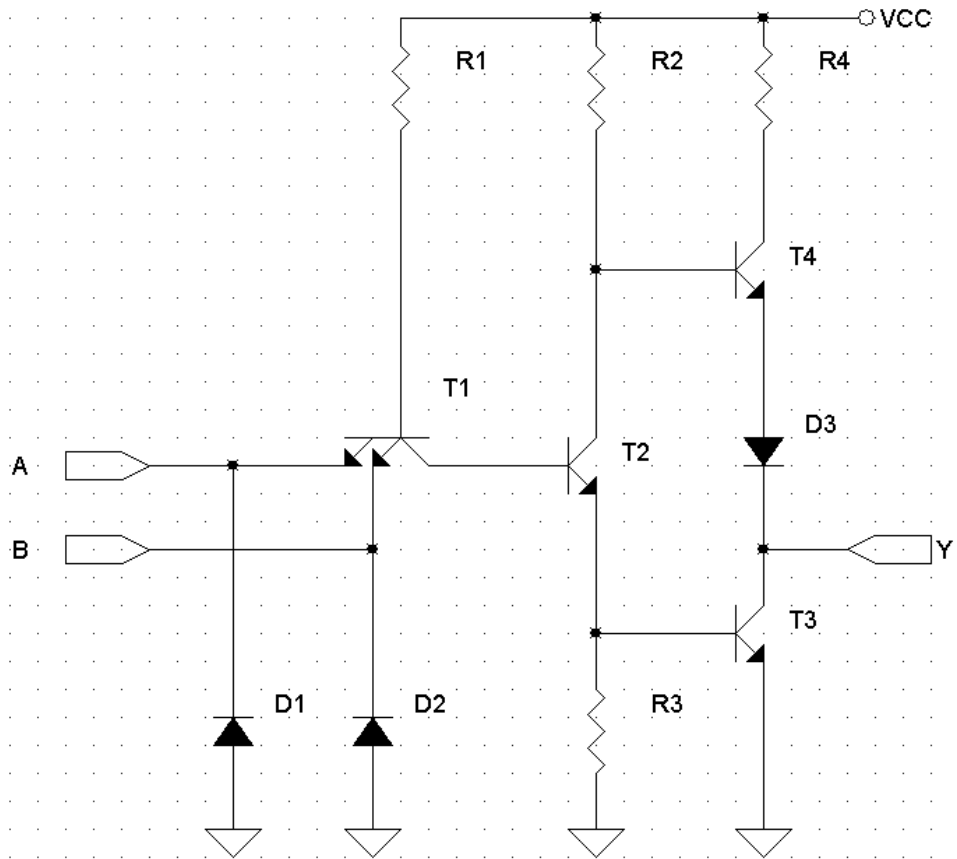
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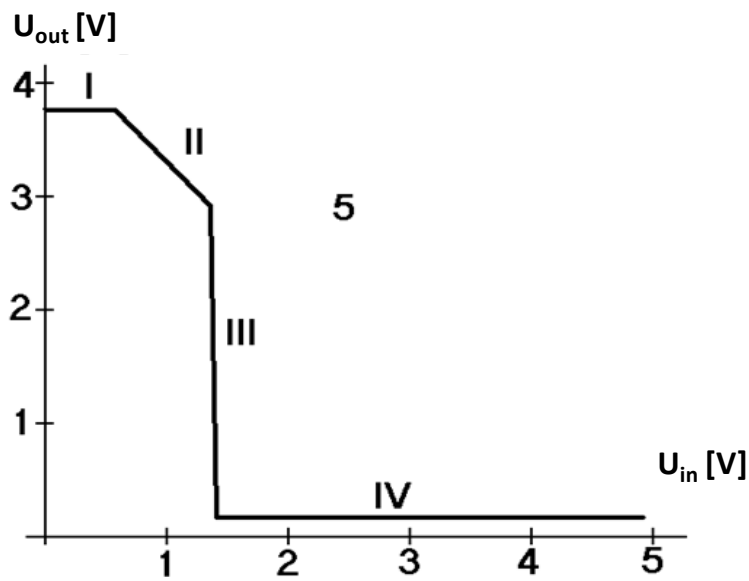

Figure 9–4.: TTL NAND gate

Figure 9–5.: Transfer characteristic of the TTL NAND gate where both of the inputs change from Logic low to logic High.

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In Phase I. both T2 and T3 is at "off" state, T4 is at "on" state. The output voltage at this time is about 3.6V due to T4 and D3. In Phase II. T2 is switched to "on", but T3 is still at "off" state, therefore the output voltage starts to drop. In Phase III. T3 also switches "on" and the circuit acts like a push-pull amplifier and the output voltage drops much faster. In Phase III. the switching point is reached, which is about 1.4V at a normal TTL gate. In Phase IV. T3, T2 is at "on" state and saturating while T4 is at "off" state. At this point the output voltage is about 0.2V.

CMOS family

The first series of CMOS devices the CD4000A appeared in the market in 1971. The CMOS series have a very low power consumption but were very slow ones. The next CS4000B series have a delay about 100ns.

Due to the improvement of technology a faster CMOS series like 74HC (High-speed CMOS) came out with a delay about 10ns.

The logic voltage levels of the CMOS ICs are significantly different from the TTL series. For example the output minimal high voltage of the CMOS series is 70% of the Vcc, which is 3.5V with high load in a 5V system, and this is lower than the TTL gates minimum input high voltage what is 3.6V. Therefore the CMOS and TTL series cannot be mixed in one system.

To solve this problem the TTL compatible CMOS series the 74HCT had been developed. In the 74HCT series the switching point is lowered to 1.4V from 2.5V to be compatible with the TTL standard.

At the later period higher speed CMOS families were introduced like 74AC (Advanced high-speed CMOS) and the 74ACT (Advanced high-speed, TTL compatible) series.

Typical design and implementation problems

Power consumption and latch-up

The power consumption of the TTL and CMOS series are very different. The CMOS series at a static state have a nearly zero power consumption, but during switching (output voltage level change from high to low, or from low to high) this increases significantly. The TTL series have a relatively high static current, and they also have a significant current peak at the low-to-high output transition, which can emit noise to the low voltage power line. Therefore the power input should be filtered with a 100nF capacitor (also recommended for CMOS series ICs).

CMOS series ICs has a vulnerability called latch-up (any CMOS series ICs not just logic gates). If a voltage level higher than the power supply plus a diode voltage or lower to the reference ground minus a diode voltage is connected to an input, or a very fast transient happened on an input line, damage of the CMOS IC may occur. This phenomena is due to the parasitic elements (parasitic capacitances, etc.) that comes from the structure of the IC.

Delays

In a complex system signals can be delayed due to many causes. There are long tracks, logic ICs and other sources of delays. In case of multiple signals the delay of the lines most likely won't be the same, which can cause problems called hazards which is out of the scope of this experiment.

Laboratory exercises 1.

Web links

http://users.ece.gatech.edu/~alan/ECE3040/Lectures/Lecture32-Basics%20of%20Digital%20Logic.pdf

http://www.asic-world.com/digital/gates4.html

http://www.asic-world.com/digital/gates5.html

http://en.wikipedia.org/wiki/Flip-flop_(electronics)

http://focus.ti.com/lit/ds/symlink/sn7404.pdf

http://focus.ti.com/lit/ds/symlink/sn7474.pdf

Measurement instruments

Digital multimeter (3½ digit)	METEX ME-22T
Power supply	Agilent E3630
Oscilloscope	Agilent 54622A
Function generator	Agilent 332220A

Test board

Evaluation board (Figure 9–6) provided for this laboratory consist of the following main parts:

- The bottom left part of the evaluation board is used for inverter circuits measurements (Figure 9–7);

- Centre part of the board is used for the D flip-flop measurement (Figure 9–8);

- An embedded pulse generator is used in flip-flop measurements as stimulus. The control knobs and signal outputs of this block is on the left part of the panel;

- The evaluation board also contains some capacitive loads, and a standard 10 gate loads (labeled as "*10 kapu terhelés*").

All of the input and output signals are accessible using standard banana plugs. Note that, high frequency signal measurement should be performed using oscilloscope probe with 10:1 or 1:100 attenuation. Therefore standard banana cables should not be used for oscilloscope connections.

The laboratory includes the measurement of several IC types. These ICs can be replaced (inverters, and flip-flops too). IC replacements are done by using the arm on the left top corner of the so called TexTool sockets. By turning the arm, ICs can be unlocked or locked. Note that the pin number 1 of inverter and flip-flop circuits always should be the pin next to the socket control arm.
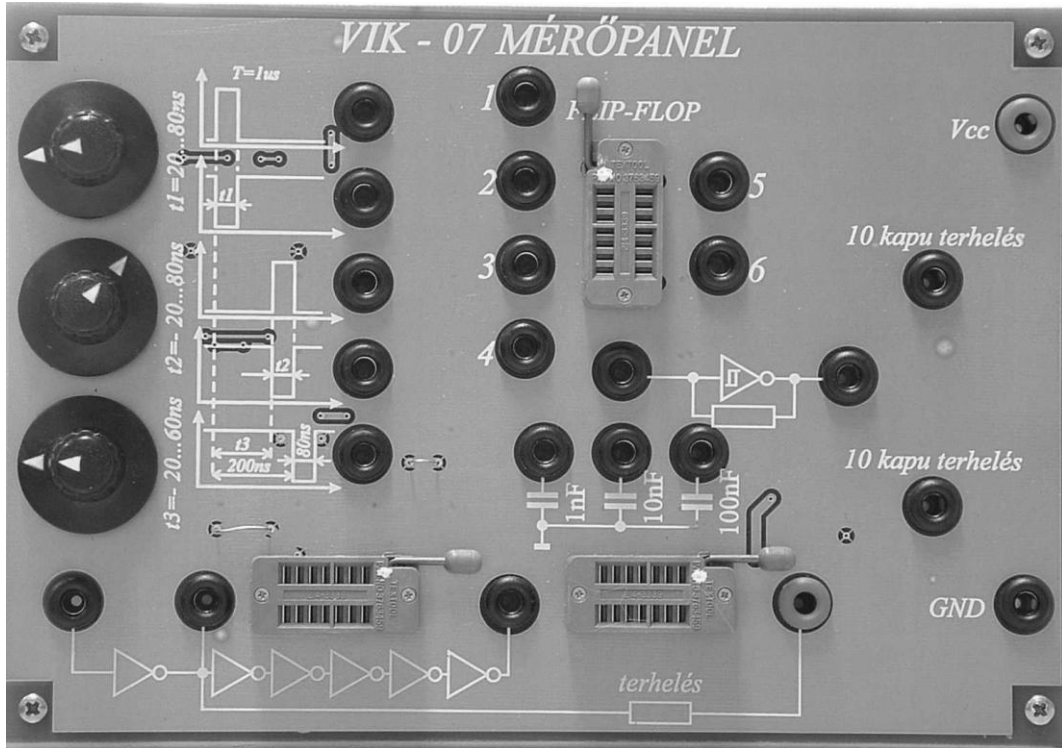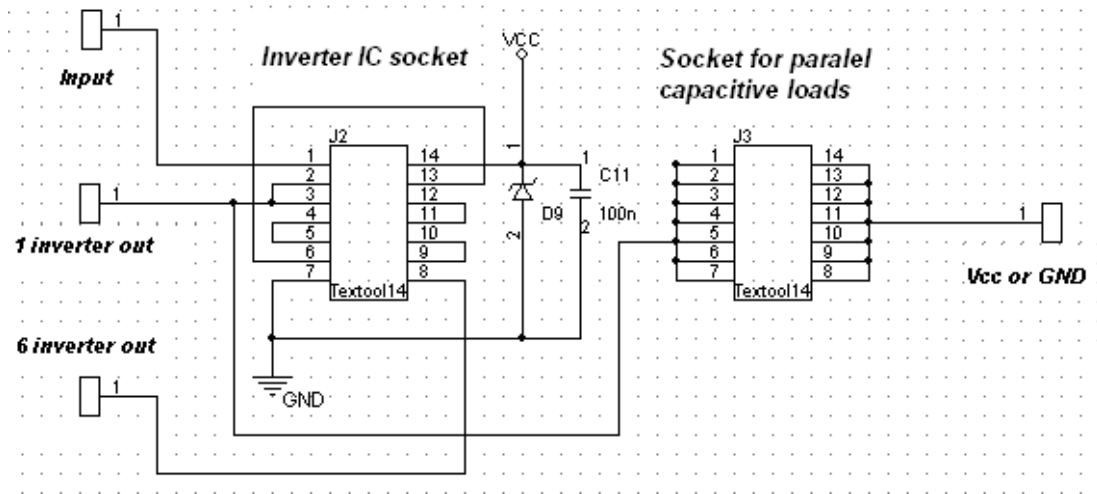
Figure 9–6.: VIK-07 Evaluation board

Figure 9–7.: Schematic of the bottom part of the evaluation board, used for inverter measurements

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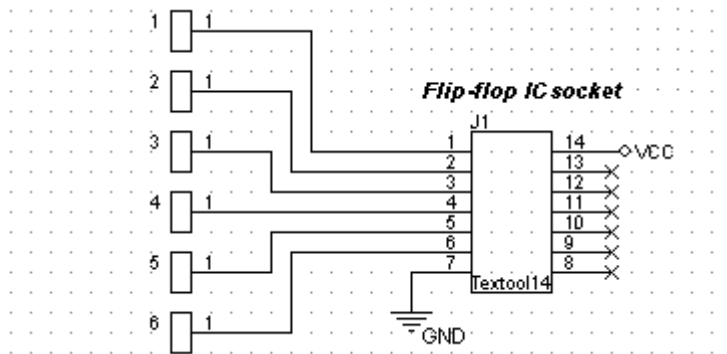

Figure 9–8.: Schematic of the center part of the evaluation board, used for flip-flop measurements
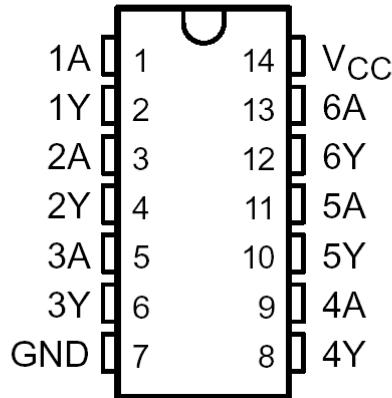
Test questions

1. What are the differences between the TTL 54 and the 74 series?

2. What are the meaning of labels L, H, LS, AS, ALS, C, HC, HCT in the names of TTL series logic circuits.?

3. Draw the internal transistor level schematic of a TTL NAND gate!

4. What is the definition of voltage transfer characteristic?

5. Draw the voltage transfer characteristic of a TTL inverter or NAND gate!

6. Which typical properties of logic gates are described in datasheets?

7. What are the voltage levels of logical **HIGH** and **LOW** levels in case of TTL and CMOS circuits.

8. What is the definition of FAN OUT?

9. What is the definition of Rise time and Fall time?

10. What is the switching point voltage of a TTL circuit?

11. What is the definition of Setup time, Hold time and Propagation delay?

12. What are the power supply range of TTL and CMOS circuits?

Pin setup of typical inverter and D flip-flop ICs

SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74S04 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)

1A	1	14 V_{CC}
1Y	2	13 6A
2A	3	12 6Y
2Y	4	11 5A
3A	5	10 5Y
3Y	6	9 4A
GND	7	8 4Y
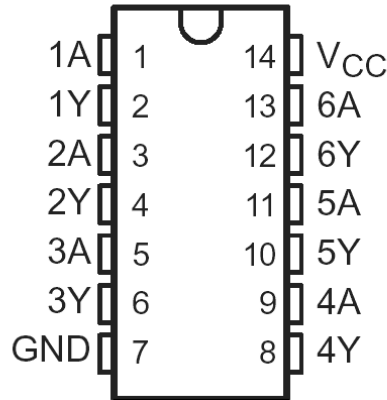
SN5414, SN54LS14 . . . J OR W PACKAGE
SN7414 . . . D, N, OR NS PACKAGE
SN74LS14 . . . D, DB, OR N PACKAGE
(TOP VIEW)

1A	1	14 V_{CC}
1Y	2	13 6A
2A	3	12 6Y
2Y	4	11 5A
3A	5	10 5Y
3Y	6	9 4A
GND	7	8 4Y

SN7474
(TOP VIEW)

1$\overline{\text{CLR}}$	1	14 V_{CC}
1D	2	13 2CLR
1CLK	3	12 2D
1$\overline{\text{PRE}}$	4	11 2CLK
1Q	5	10 2$\overline{\text{PRE}}$
1$\overline{\text{Q}}$	6	9 2Q
GND	7	8 2$\overline{\text{Q}}$