ARM Cortex core microcontrollers

5th Basic peripherals of microcontrollers

Balázs Scherer

Budapest University of Technology and Economics
Department of Measurement and Information Systems

Topics

- General purpose I/O pins
- Timers
- SPI
- I2C
- UART
- ADC, DAC
- CAN

GPIO pins

- Present in microcontrollers sine 1970s
- Organized to ports:
  - Can be 8-bits, 16-bits, or 32-bits ports

- Electrical characteristics
  - Max, min power supply:
    - Logical 0: usually max. 0.1V
    - Logical 1: usually min. Vcc*0,7
    - 5 Volt tolerant pins or not?
  - Maximal load and sink current
    - Usually: 10mA, less usual 4mA
    - Sink currents are usually higher: 20mA
  - Timing
    - One cycle, or peripheral clock depended behavior

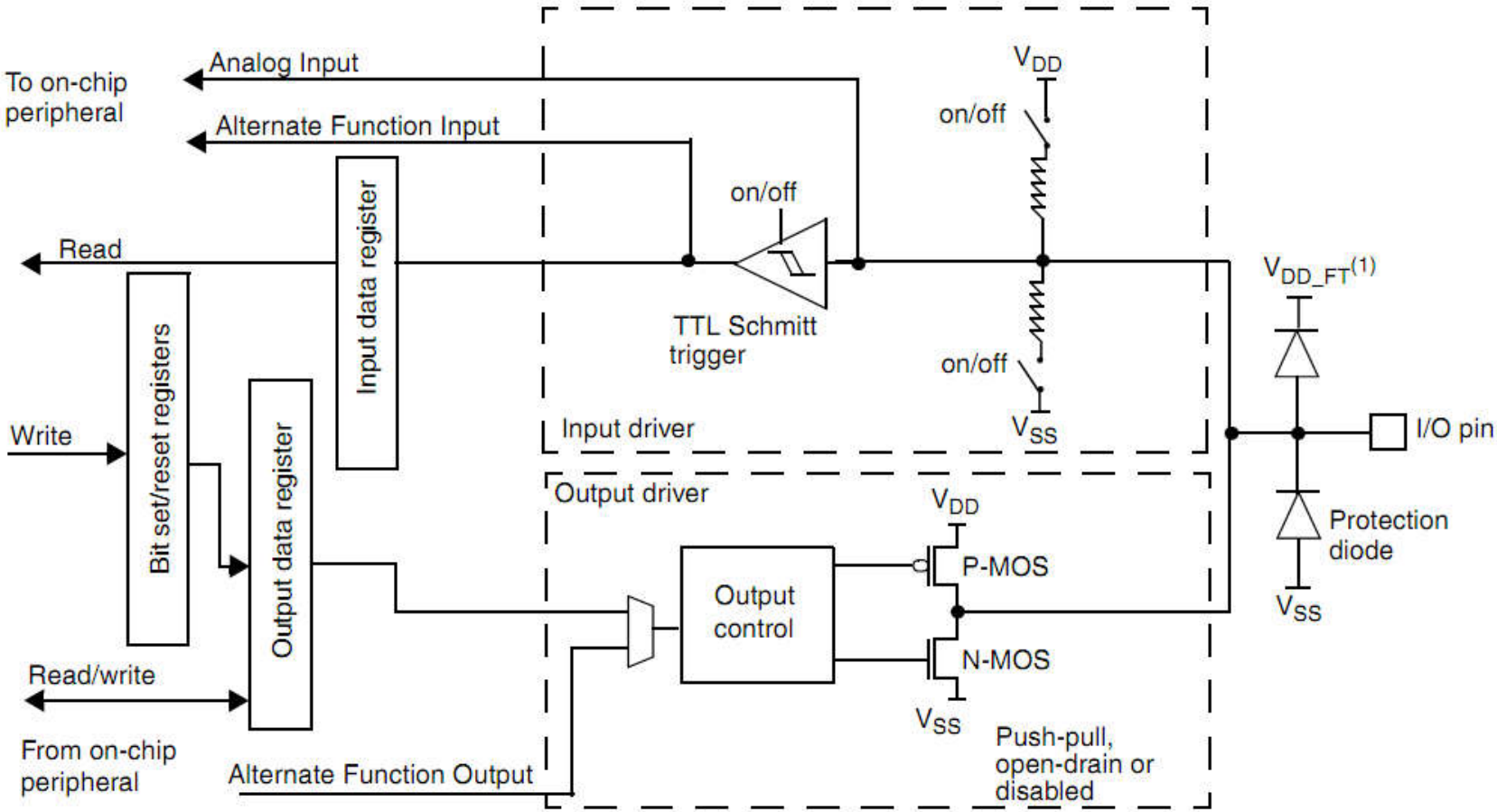
GPIO pins

- A port has at least 3 registers
  - PIN direction
  - Data Write
  - Data Read

- Today micros make them more configurable
  - Port function registers
    - Alternate function
    - Driving type: push-pull, open drain
    - Pull up, Pull down configuration

GPIO pins

- A modern I/O block (STM32F)



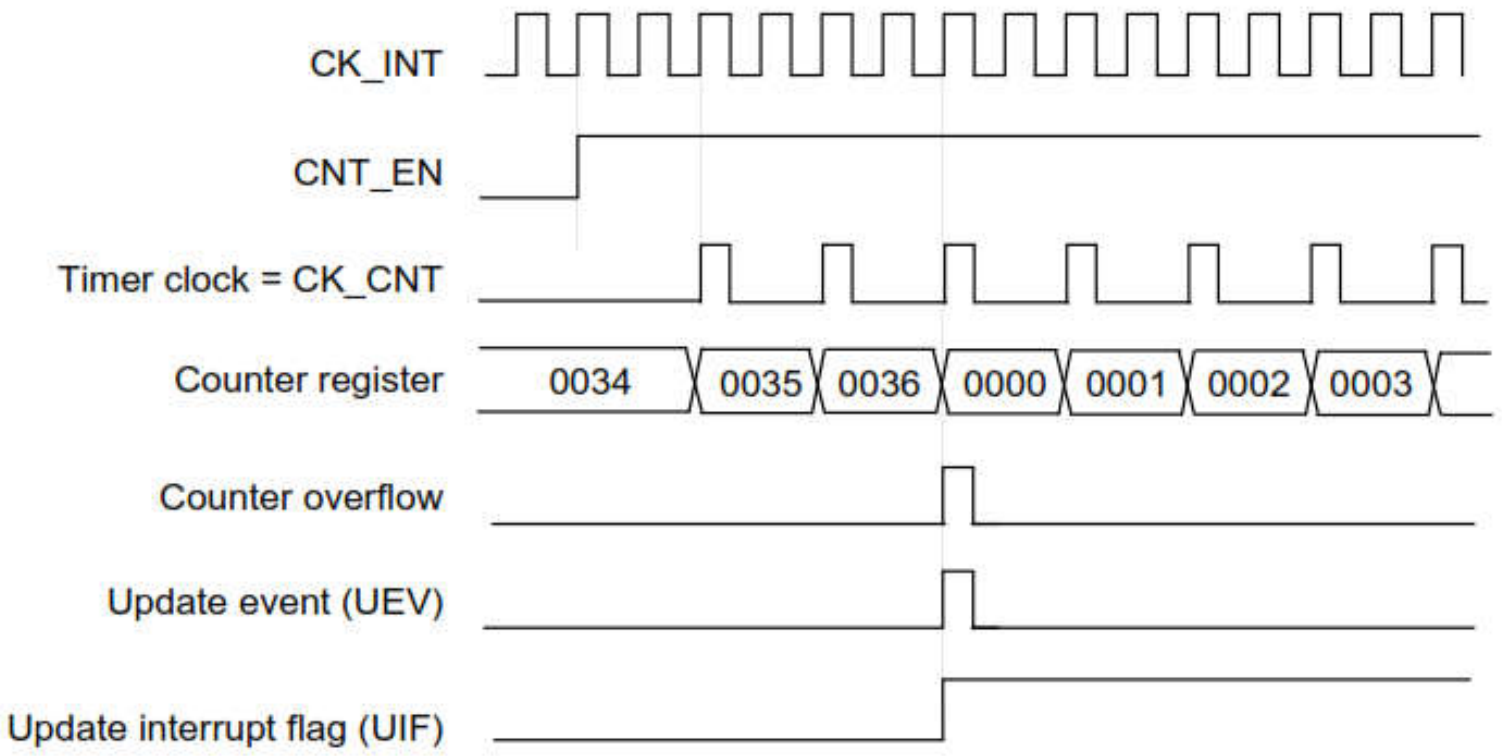
Timers

- Present since the first micros
- 8,16,32 bit versions
- Many choices to
  - System clock
  - Dedicated crystal
  - External event
- Basic functions
  - Selectable prescaler
  - Up or down counting
  - Clear, reload
  - Automatic roll over, or stop on overflow
  - Interrupt request

Timers: the prescaler

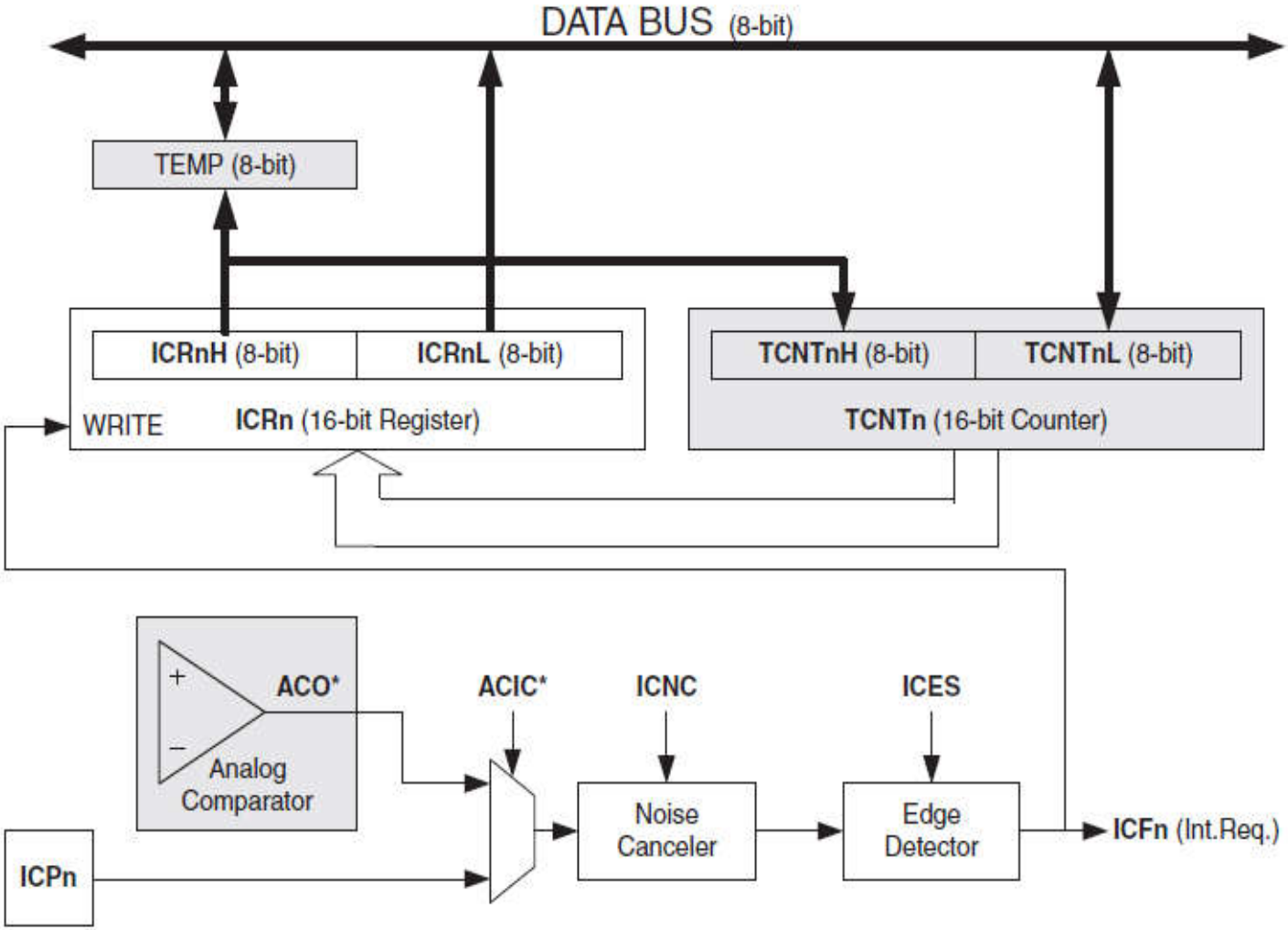
- Prescaler in work: example counter counts util 36

Figure 138. Counter timing diagram, internal clock divided by 2



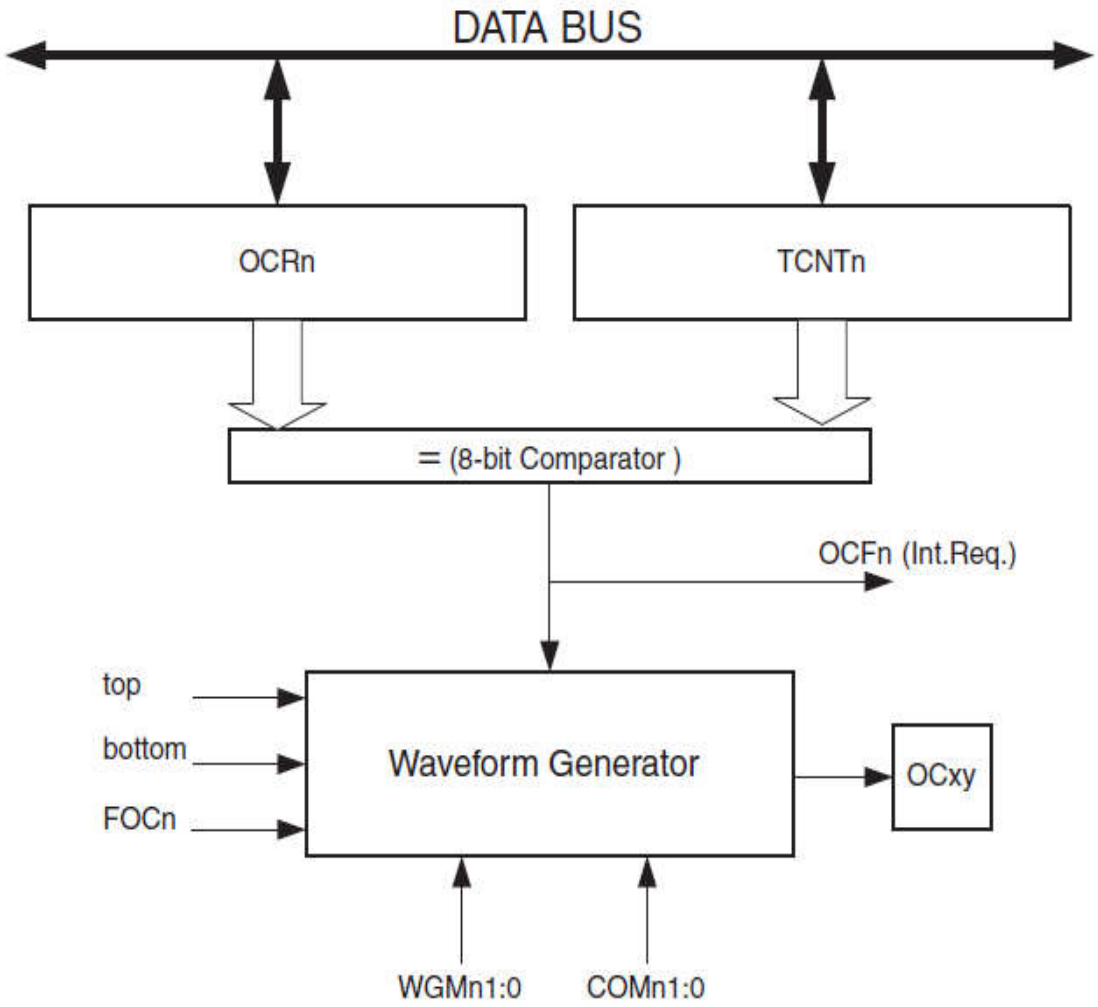
Timers: extended functionality

- Input capture



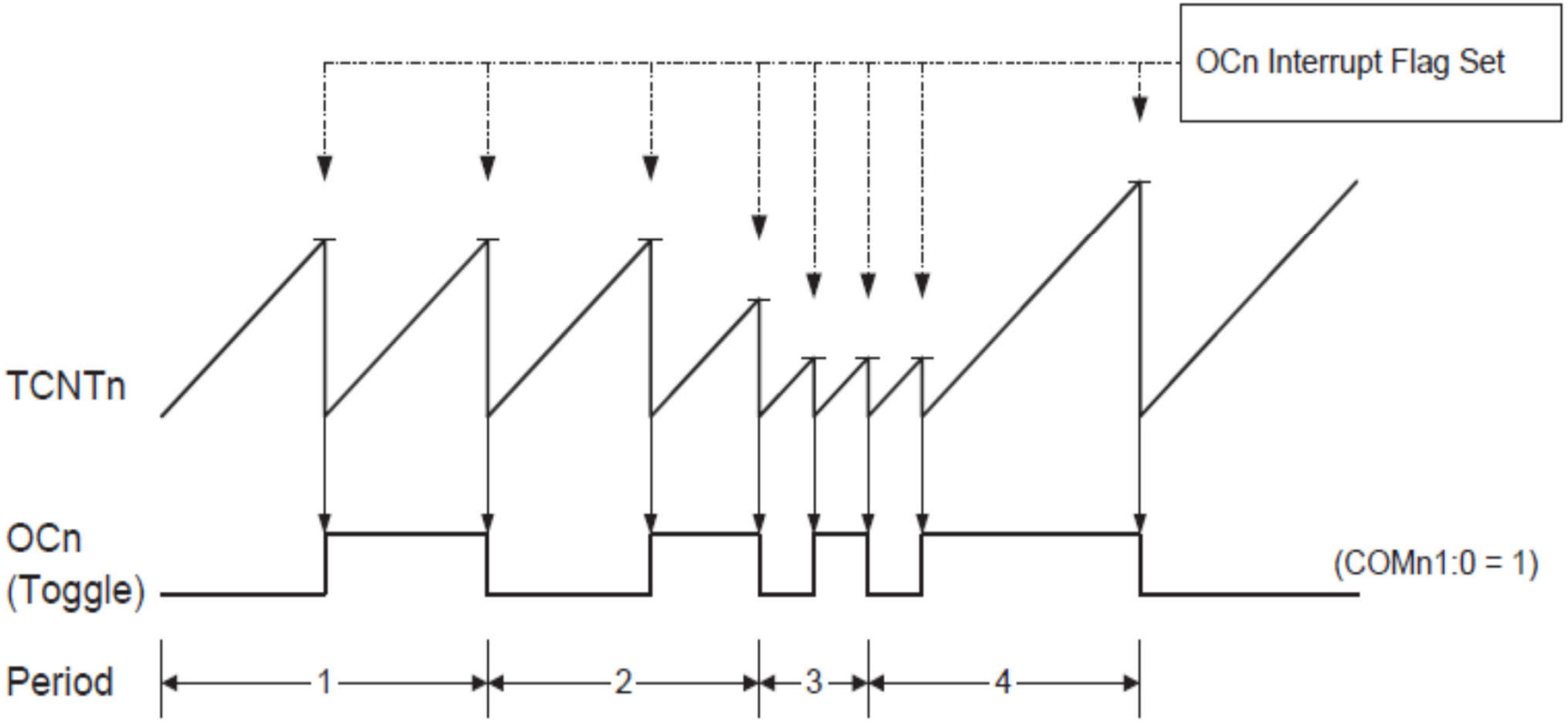
Timers: extended functionality

- Compare Output



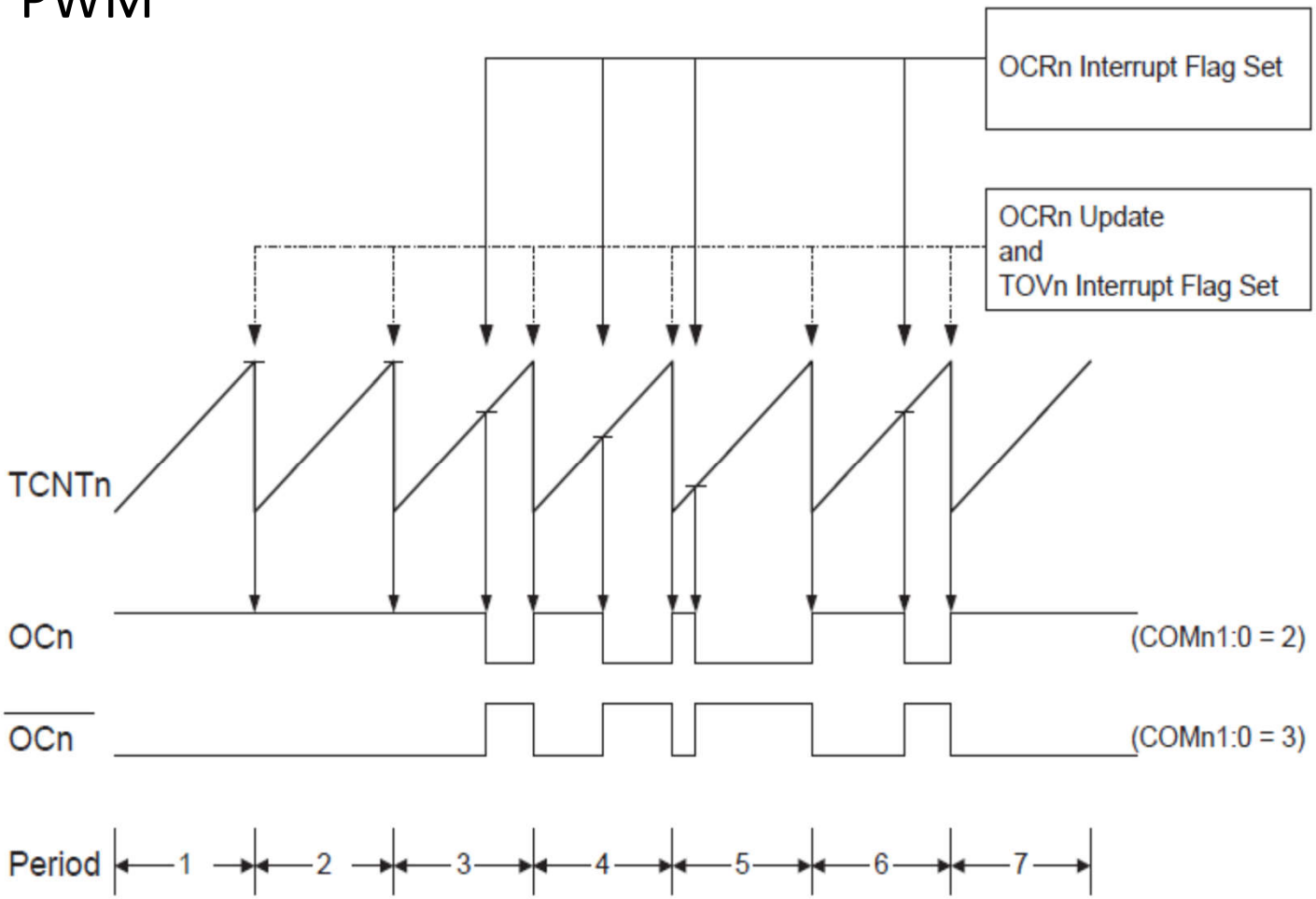
Timers: extended functionality

- Compare Output



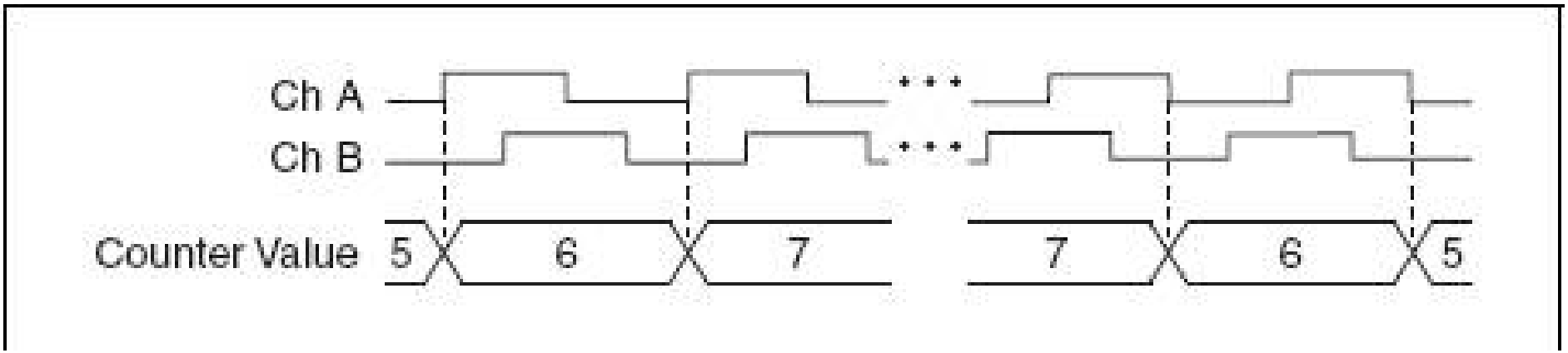
Timers: extended functionality

- PWM



Timers: extended functionality

- Encoder interface

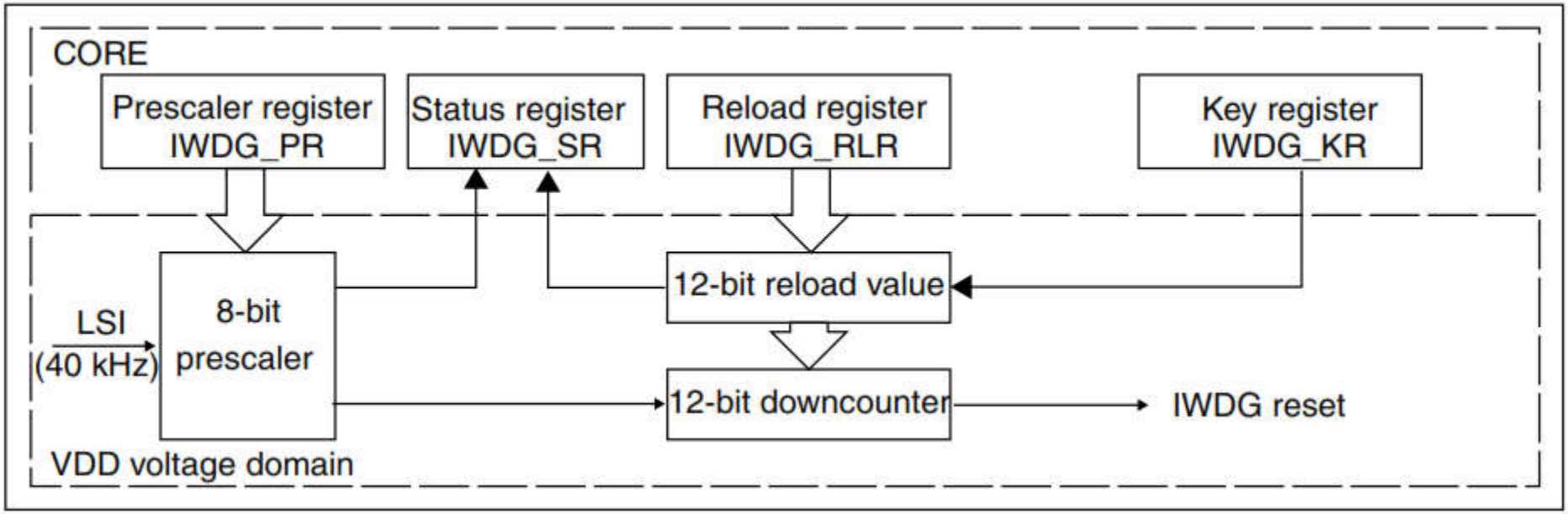


Timers: extended functionality

- Motor Control PWM-s
  - Optimalised to control 3 phase BLDC motors
  - Timer Arrays
    - Connecting timer
- Real-Time Clock
  - Dedicated 32.768 kHz crytal
  - Separate power domain
    - Separate battery
  - Calendar functionality
  - Alarm possibilities
    - Able to wake the microcontroller from sleep

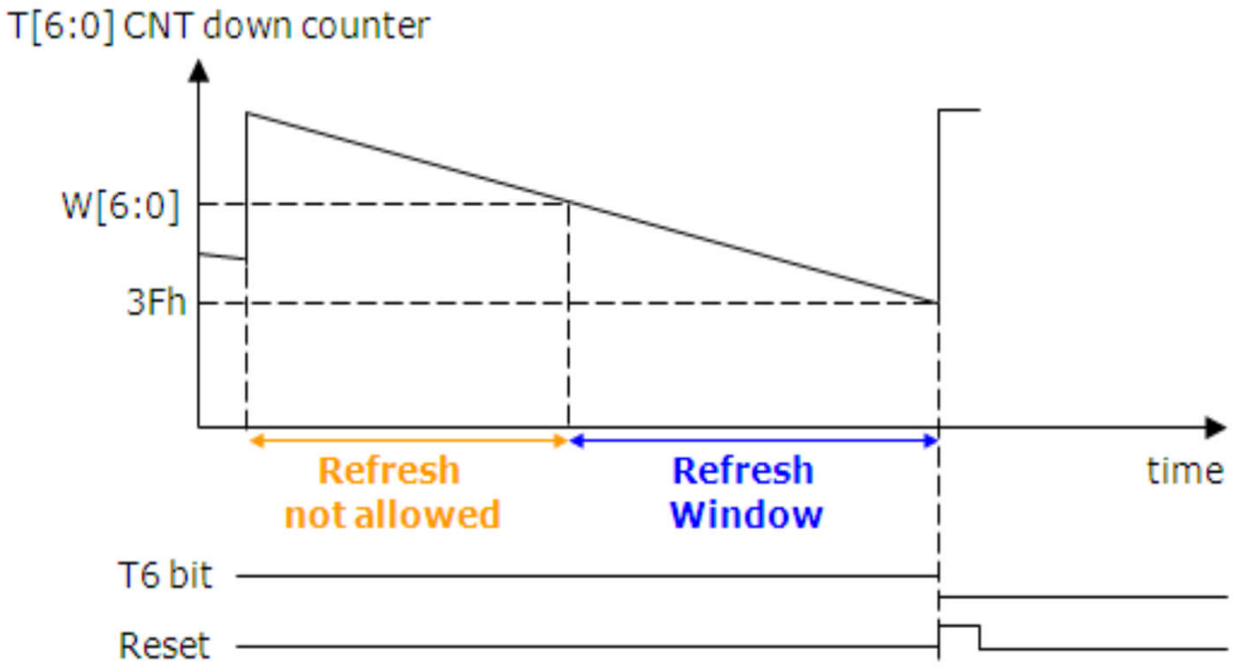
Timers: extended functionality

- Watchdog timer
  - Reset the microcontroller at overflow
  - Independent clock source
  - What happens during debug?



Timers: extended functionality

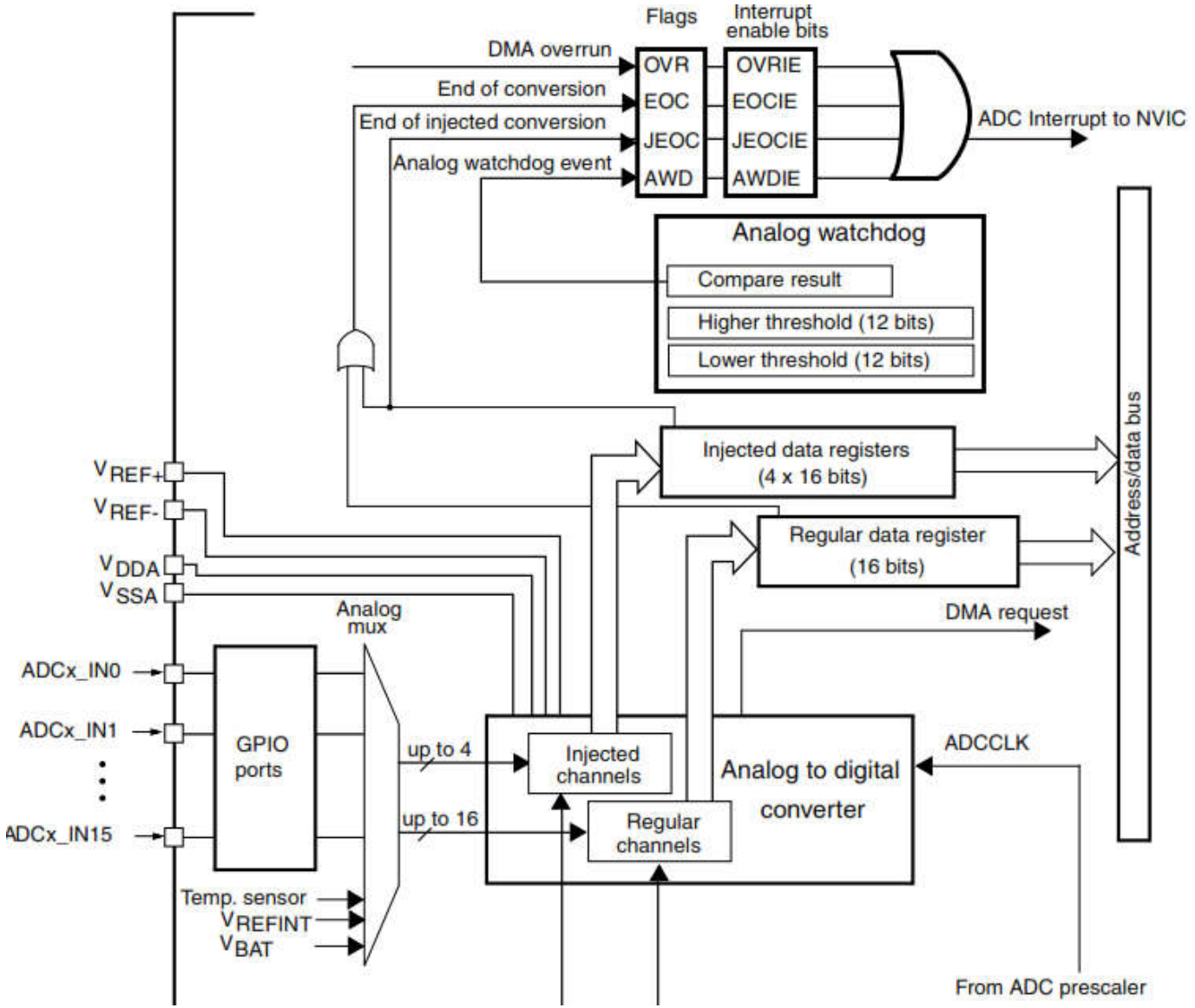
- Windowed watchdog timer
  - Windowed mode: there is a window where the refresh is possible



ADC: Analog to Digital Converter

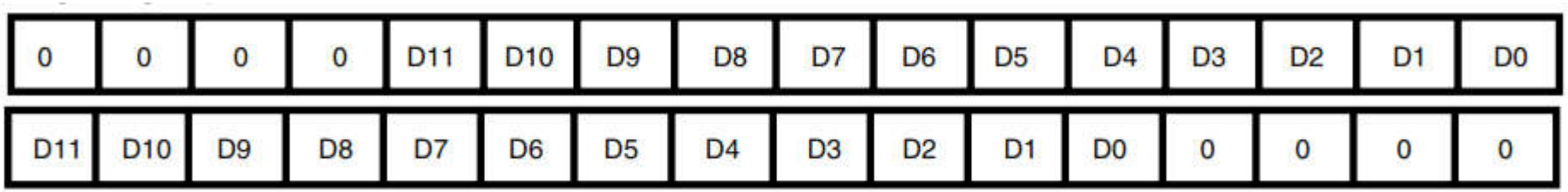
- Separate power pins
  - Should be separated during the PCB design
- Reference:
  - Power supply
  - Internal 2.56V
  - External
- Usually 10 or 12 bit (successive approximation AD)
  - Rare microcontroller lines with 16-bit ADC
- Alternate functionality of GPIO pins
- 1 or two ADC with multiple channels
- Conversion peed up to a few MSample/sec

ADC: Analog to Digital Converter



ADC: Analog to Digital Converter

- Data accessing

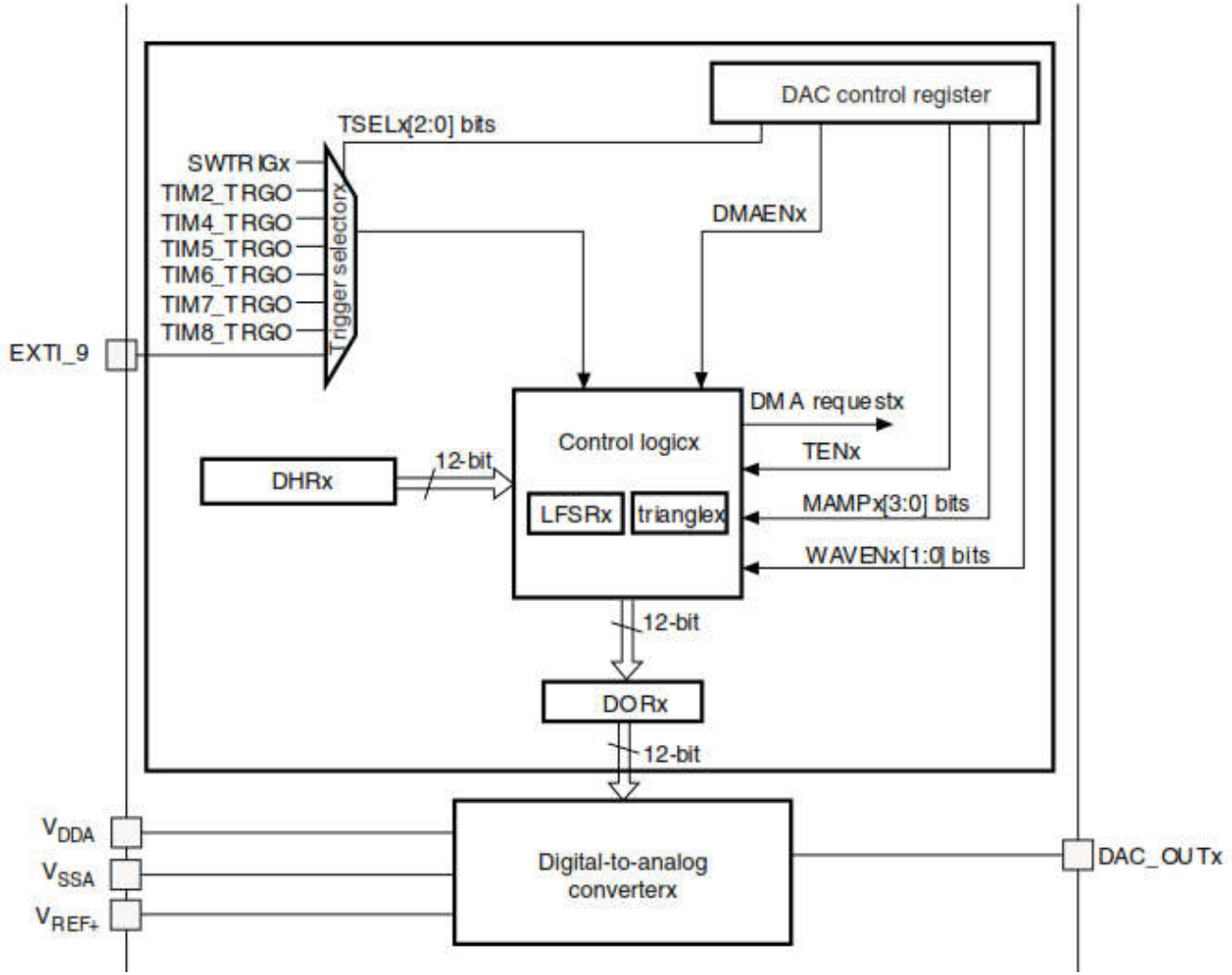


0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0

- Syronisating multiple ADCs

DAC: Digital to Analog Converter

- Many times can be used for generating a wave form

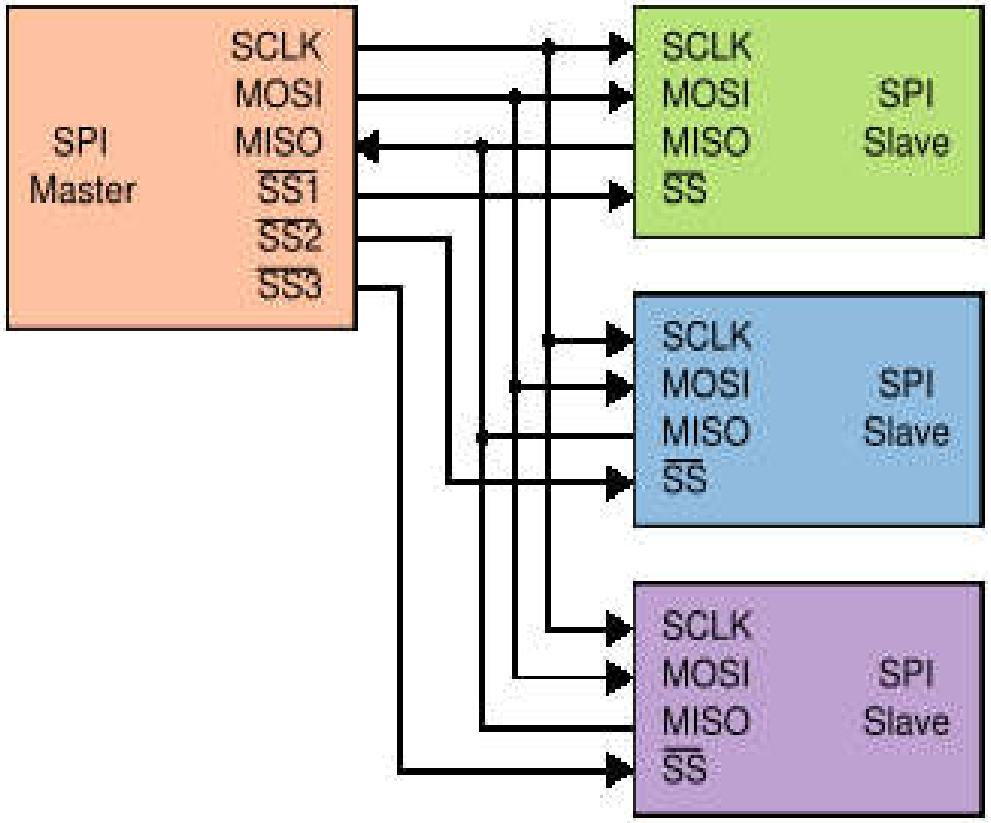


SPI: Serial Peripheral Interface

- Developed by Motorola
- Master – Slave architecture
- 4 wire communication
  - SSEL: Slave Select
  - SCK: Serial Clock
  - MOSI: Master Out Slave In
  - MISO: Master In Slave Out
- Synchron data transfer
  - Riseing or falling edge sampling
- Rather fast full-duplex communication
  - SCK rate can be high (n * MHz)

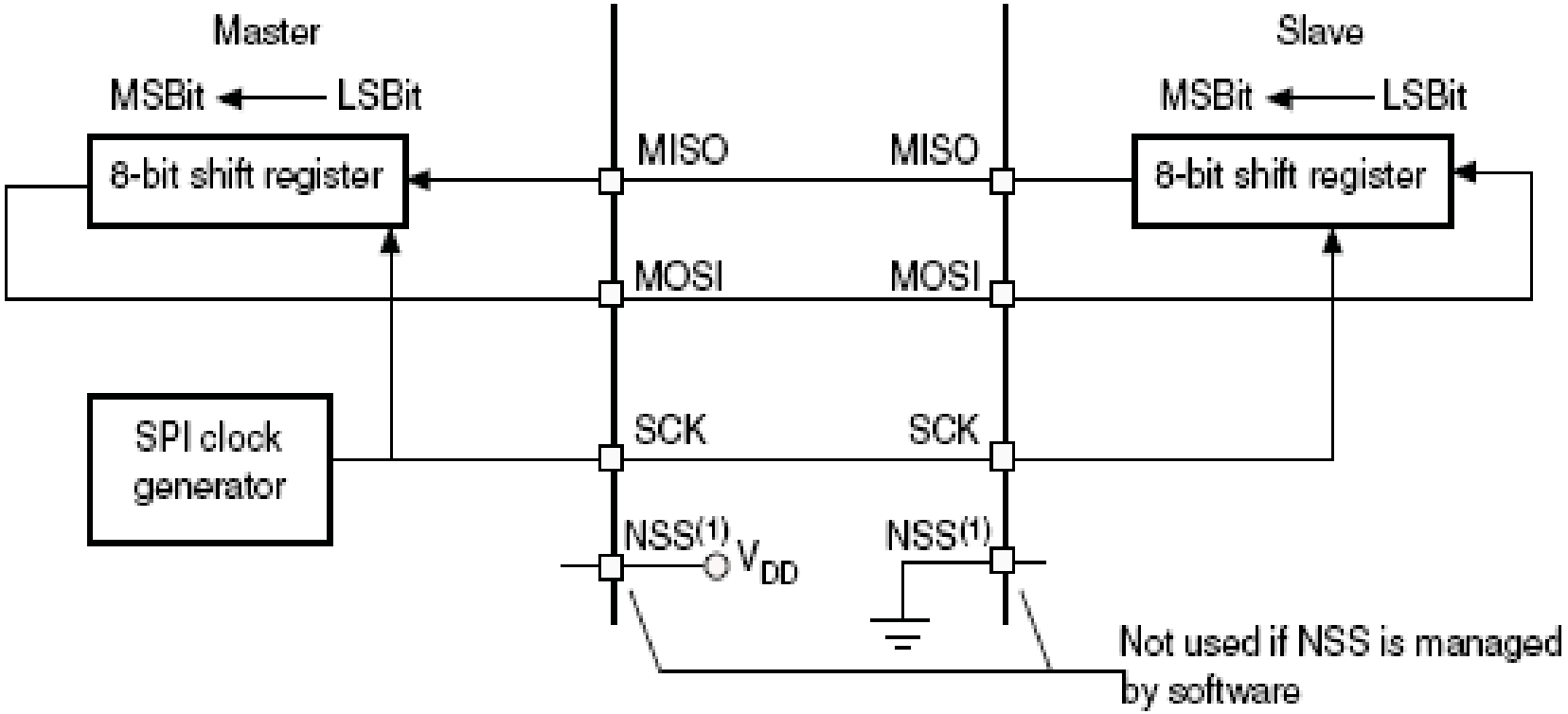
SPI: Serial Peripheral Interface

- Master – Slave architecture



SPI: Serial Peripheral Interface

- Data transfer



SPI: Serial Peripheral Interface

- Peripherals using SPI
  - ADC, DAC
    - Easy galvanic isolation
  - EEPROM-s
  - Sensors
    - Temperature
    - Acceleration sensor
  - Communication controllers
    - CAN, ZigBee
  - Some graphical LCD-s

SPI in 32 bit microcontrollers

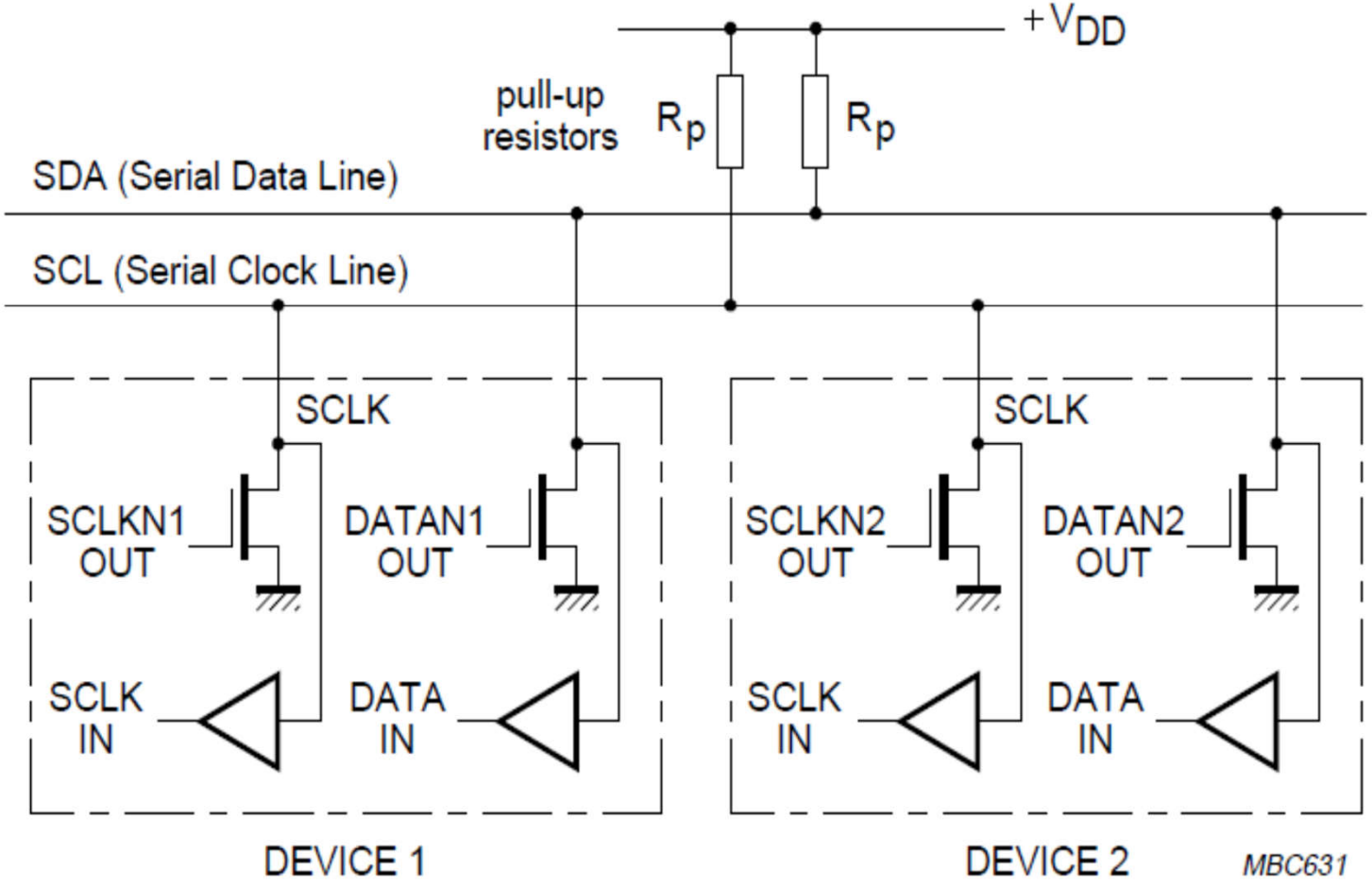
- STM32F107
  - Max. 18MHz full-duplex, 8-, 16-bit blokks
    - DMA for transmit and receive
  - Hardware supported CRC8, CRC16 calculations
    - Good for MMC, SD card handling
- LPC18xx Quad SPI interface
    - 1,2,4 bit operation
    - Max. 54 Mbit/sec

Inter-Integrated Circuit: I2C

- First version announced in 1992
- Two wire, half-duplex communication
  - SCL: Serial Clock Line
  - SDA: Serial Data Line
- Usually 1 master many slave, but possible to use with many masters
- Maximum node number is determined by bus capacitance (400pF)
- Data rate
  - 100kbps (standard)
  - 400kbps (fast)
  - 3,6Mbps (high-speed)
- 7-bit or standard 10-bit extended addressing

Inter-Integrated Circuit: I2C

- Physical layers
  - Logical 1: Vdd, Logical 0: GND

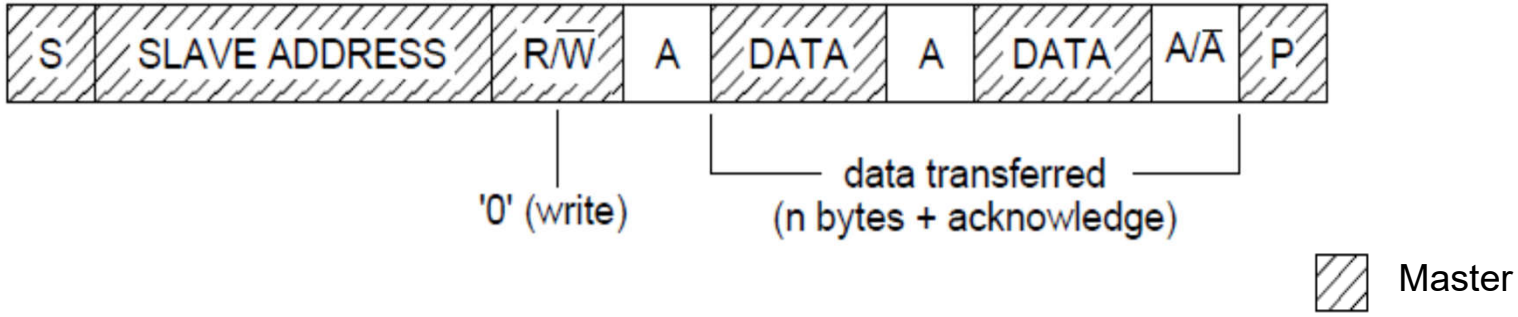


Inter-Integrated Circuit: I2C

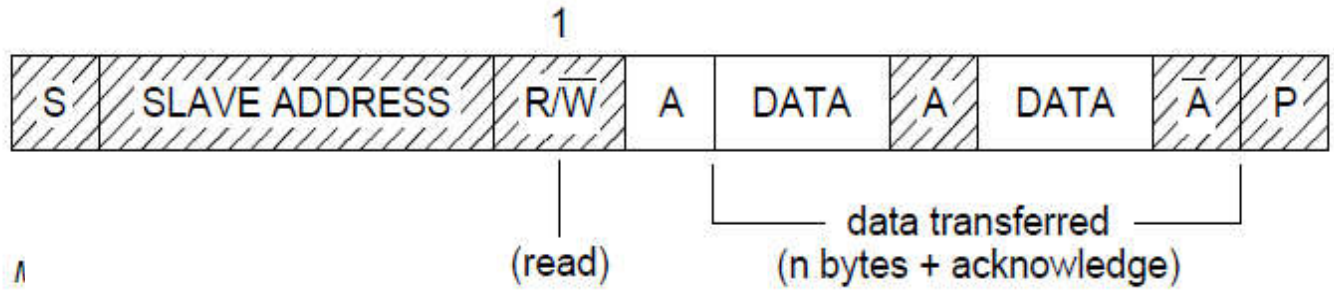
- Communication stat with the Start condition
- The SCL signal driven by the Master
- The SDA cannot change during the high state of SCL (data transfer)
- Byte based transfer 8 bit + ACK bit
- The MSB bit is transmitted first
- Address byte, then data bytes
- If there are multiple masters, then arbitration is done (wired AND)

Inter-Integrated Circuit: I2C

- Data transfer
  - Writing



  - Reading

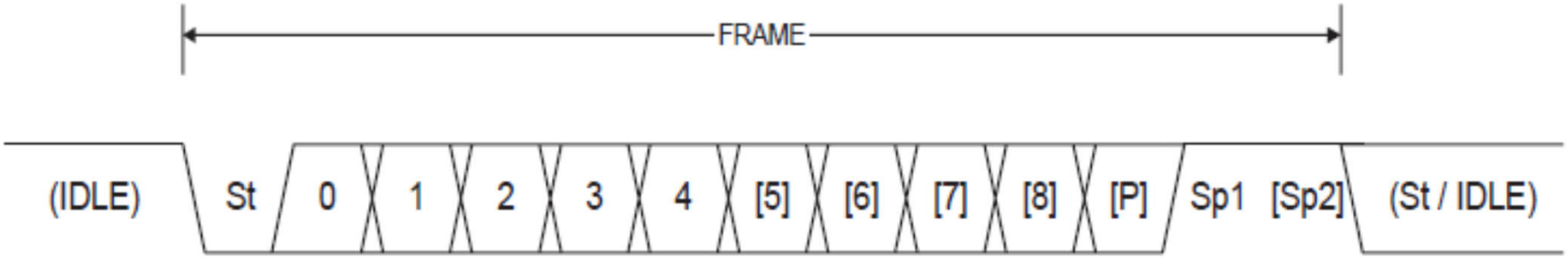


Inter-Integrated Circuit

- Typical peripherals with I2C interface
  - Low channel count ADC, DAC
  - EEPROMs
  - Sensors
    - Temperature
    - Humidity
    - Pressure
  - Port extenders

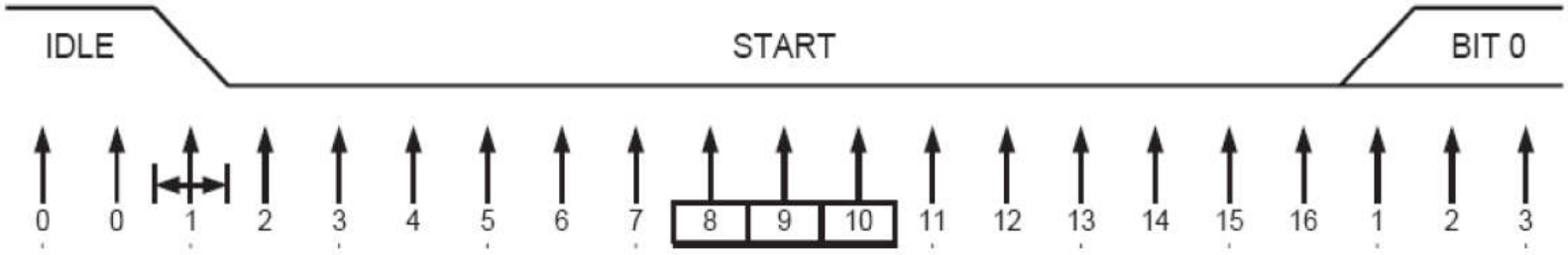
Universal asynchronous receiver/transmitter: UART

- Asynchronous communication
- UART frame
  - Start Bit
  - 5, 6, 7, 8 or 9 data bit
  - Parity Bit
  - 1, 1.5 or 2 Stop Bit
- Standard Date rates: 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200



UART

- UART physical layer: bit sampling
  - Sampling start at the falling edge of the start bit
  - Bit synchronization should keep during one frame
  - Clock rate differences between transmitter and receiver could cause problems (Temperature for RC oscillator)
    - More than 2% difference to the nominal clock rate can cause problem (try to keep difference <1%)



UART

- Examples for UART interfacing
  - PC terminal, debug, measurement device control (Rs232)
  - Industrial network (Rs485)
  - IrDA
  - Automotive communication
    - LIN (Local Interconnect Network)
  - Interfacing to communication modems
    - GSM, GPS, GPRS modem
    - ZigBee
    - TCP/IP chip
    - Wi-Fi interface
    - Power Line communication
    - USB virtual com port

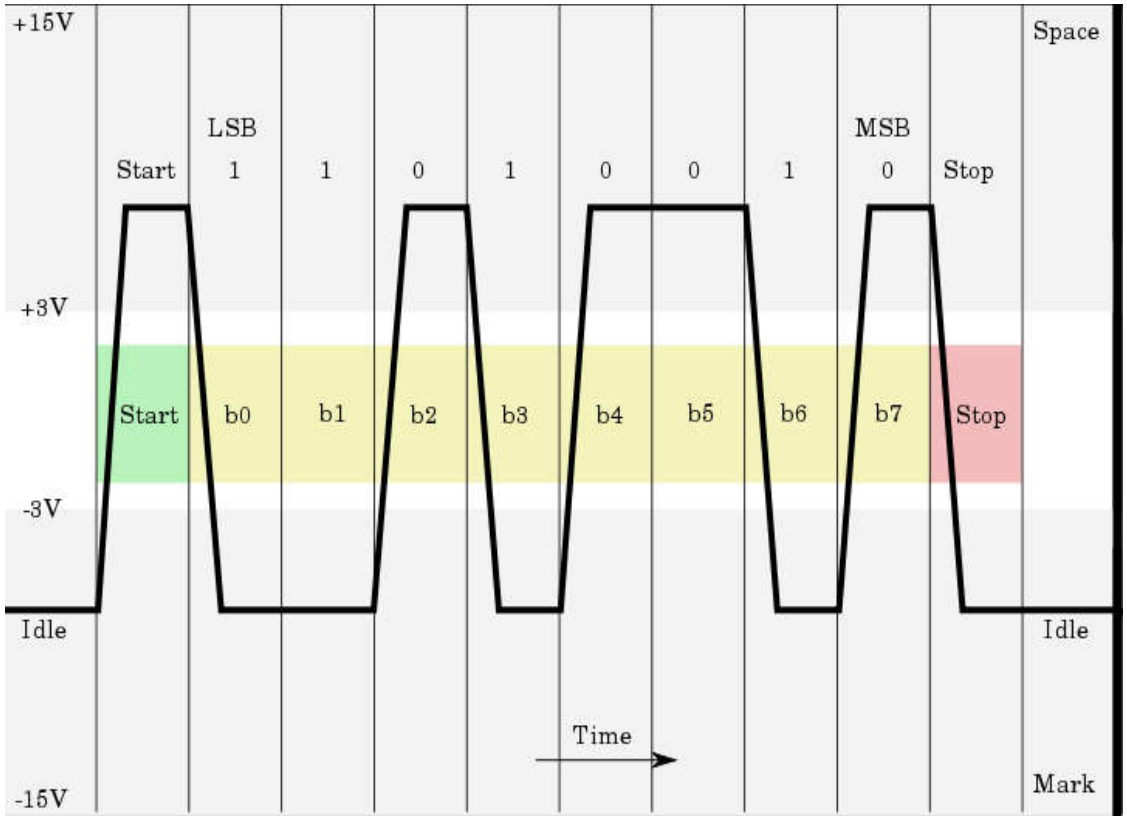
Rs232 (EIA Standard RS-232-C)

- Physical layer

Logic level	Transmitter	Receiver
0	+5...+15	+3…+25
1	-5…-15	-3…-25

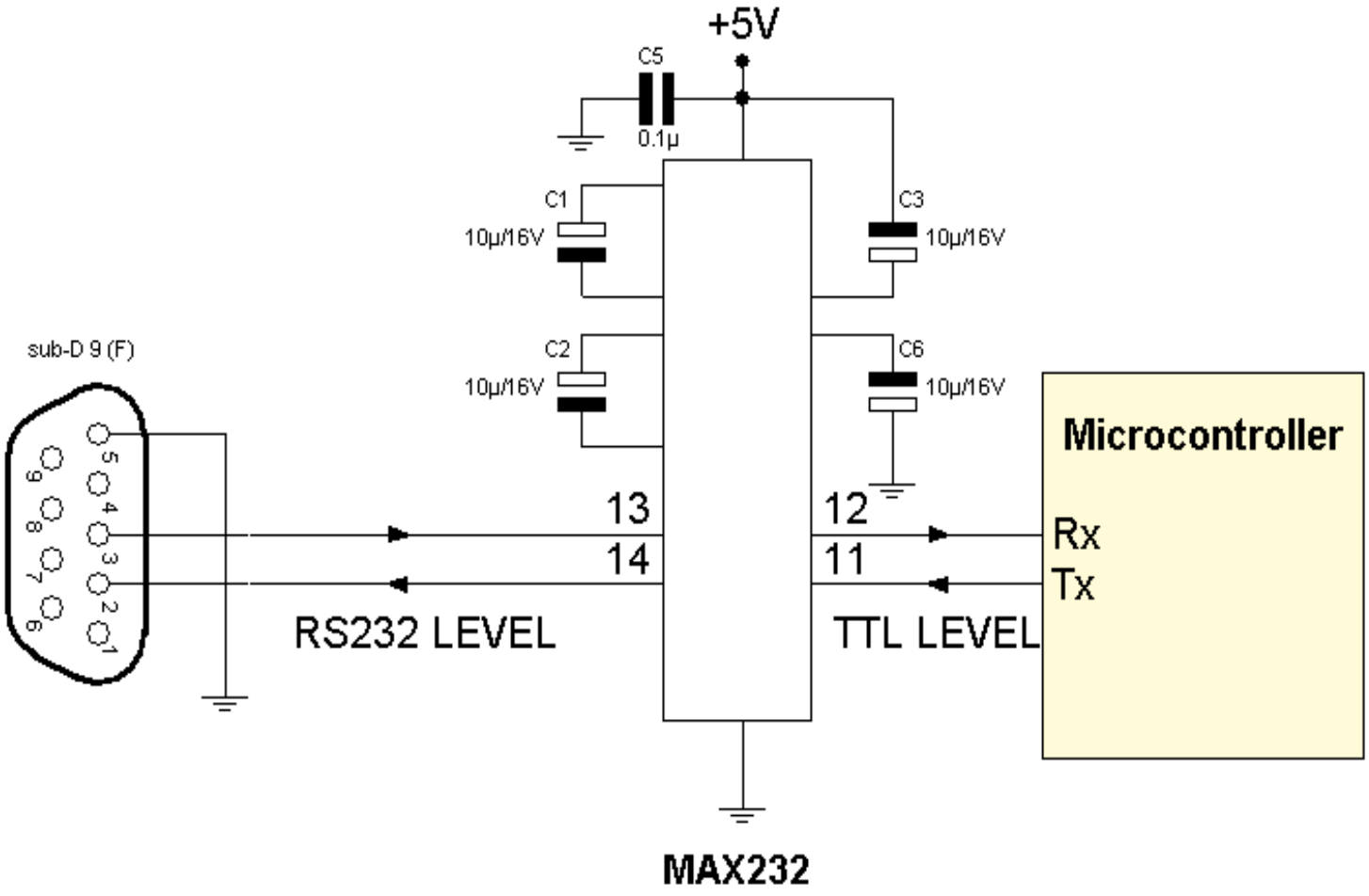
- Range

Baud rate	Kábelhossz (kb)
19200	15m
9600	150m
4800	300m
2400	1000m



Rs232 (EIA Standard RS-232-C)

- Rs232 connection: microcontroller – PC conection

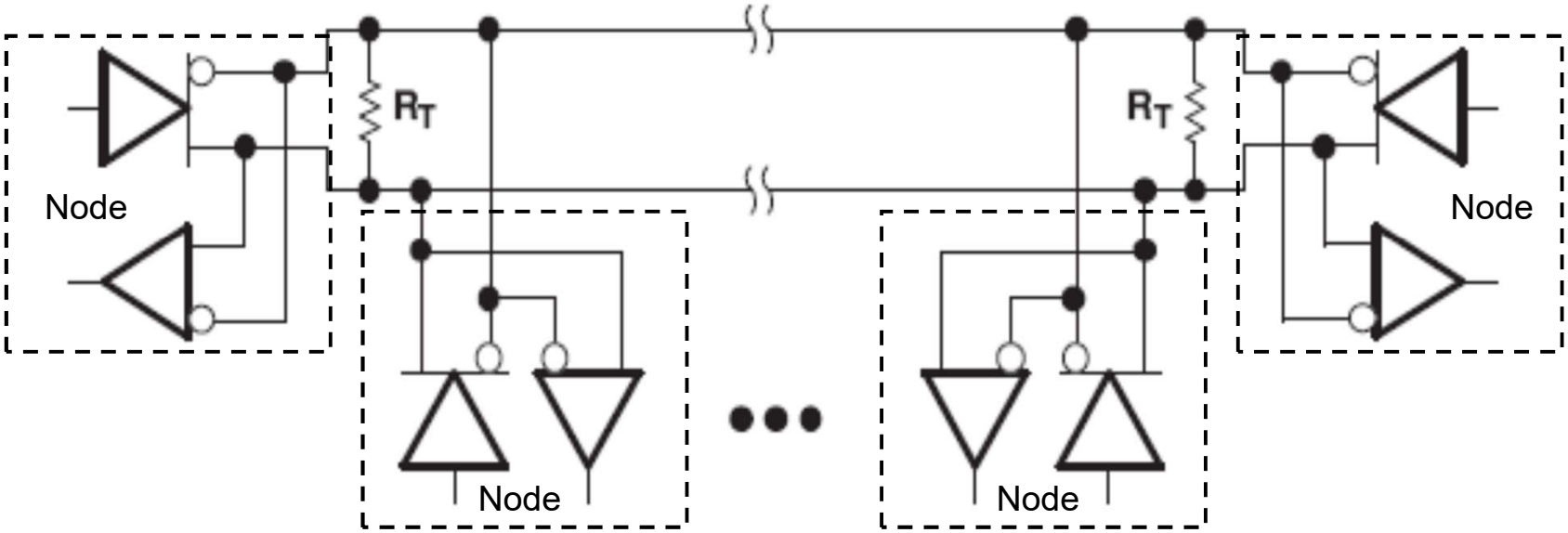


Rs485 (EIA-485)

- Bus architecture
  - maximum 1200m range
- Standard describe only the Physical layer
- No rules for addressing, collision detection …
- Twisted pair wiring with differential balanced signaling
  - Termination resistor is used
- Half-duplex transfer
  - Usually master-slave architecture
- Can be used in full-duplex mode with 4 wires

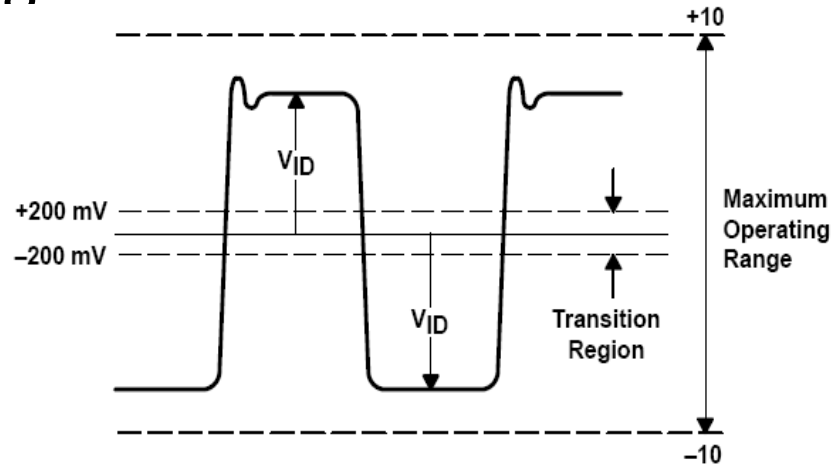
Rs485 (EIA-485)

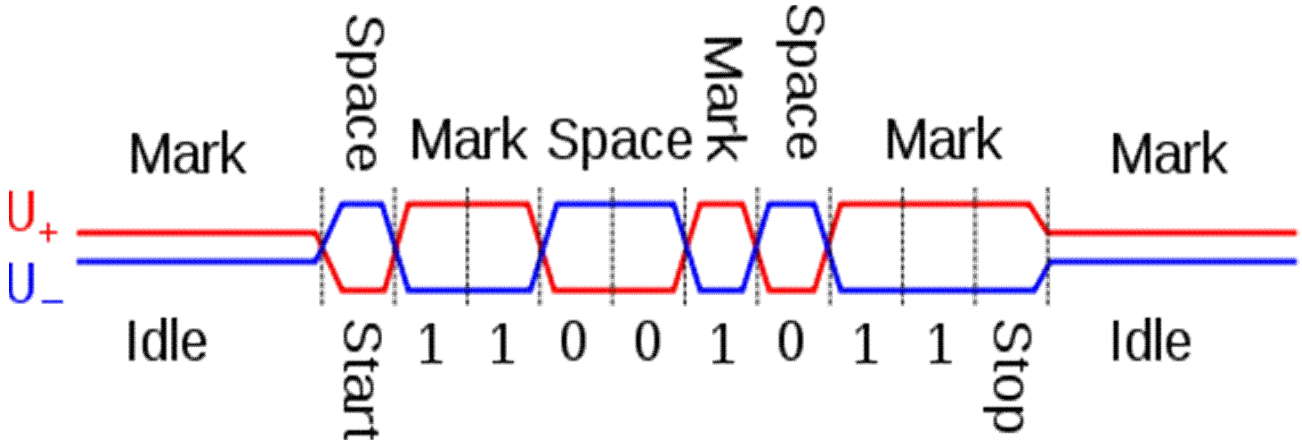
- Physical layer



Rs485 (EIA-485)

- Logical levels and Physical voltages
  - Differential signaling
    - **A** is the **inverted** or '-' signal
    - **B** is the **non-invertied** or '+' signal





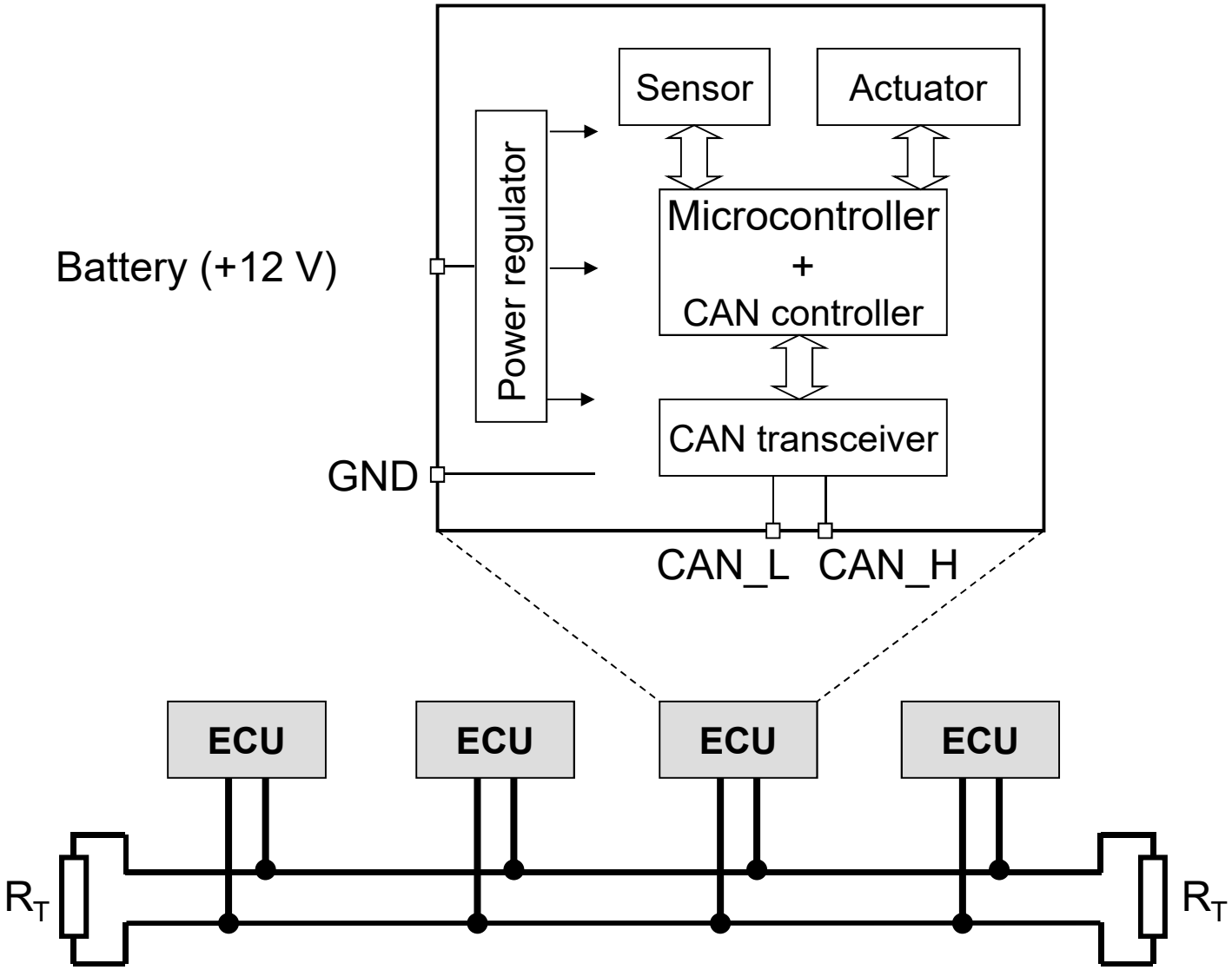
Rs485 (EIA-485)

- Application: One of the cheapest industrial bus system
  - Nowadays industry prefers CAN or Ethernet more
    - They have data-link layer suppor
- PLC-s
- Modbus
- Profibus

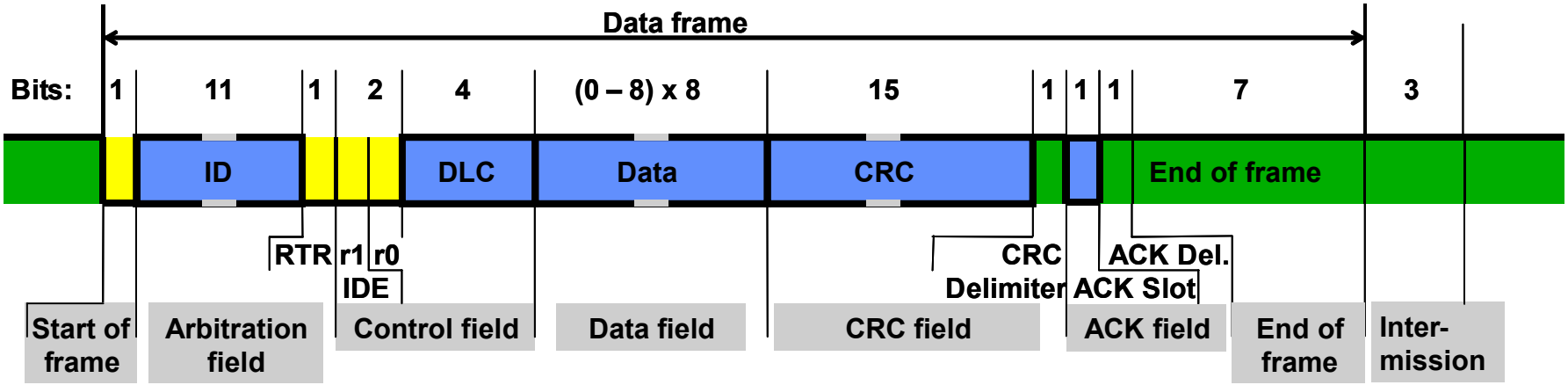
CAN: Controller Area Network

- Maximum 1 Mbit/s communication data rate
  (low speed: 10 kbit/s - 125 kbit/s-ig,
  High-speed: 125 kbit/s - 1 Mbit/s, usually 500 k)
- Range:
  - 100 m (330 ft), 500 kbit/s
  - 200 m (650 ft), 250 kbit/s
  - 500 m (1600 ft), 125 kbit/s
  - 6 km (20000 ft), 10 kbit/s
- Usually twisted pair cable used as physical media
- Non-Return to Zero (NRZ) bitcoding with bit-stuffing
- Short variable length data frames (0–64 bit data frame)

A CAN network



Data frame – 2.0A / Standard CAN

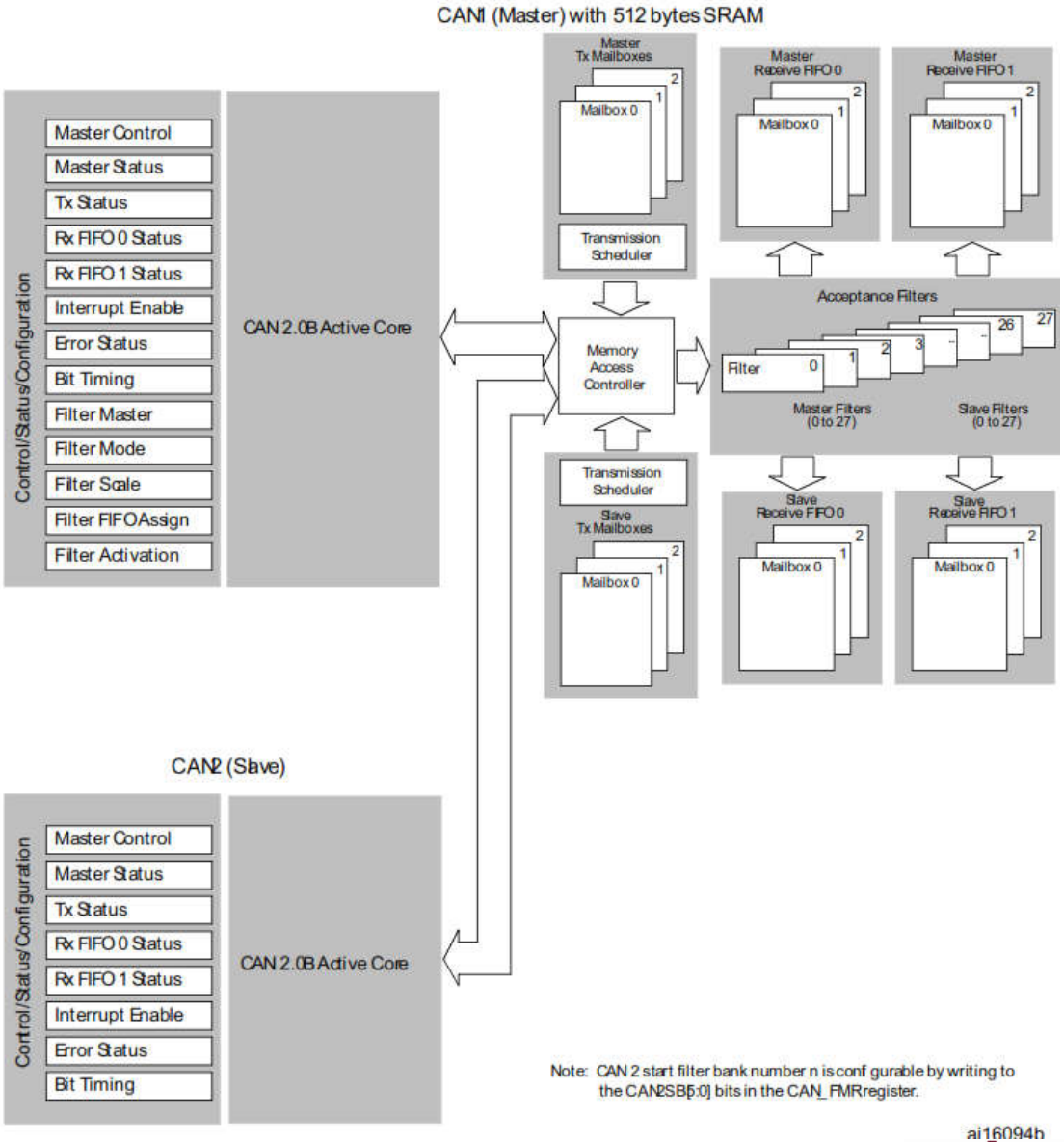


= recessive

= dominant

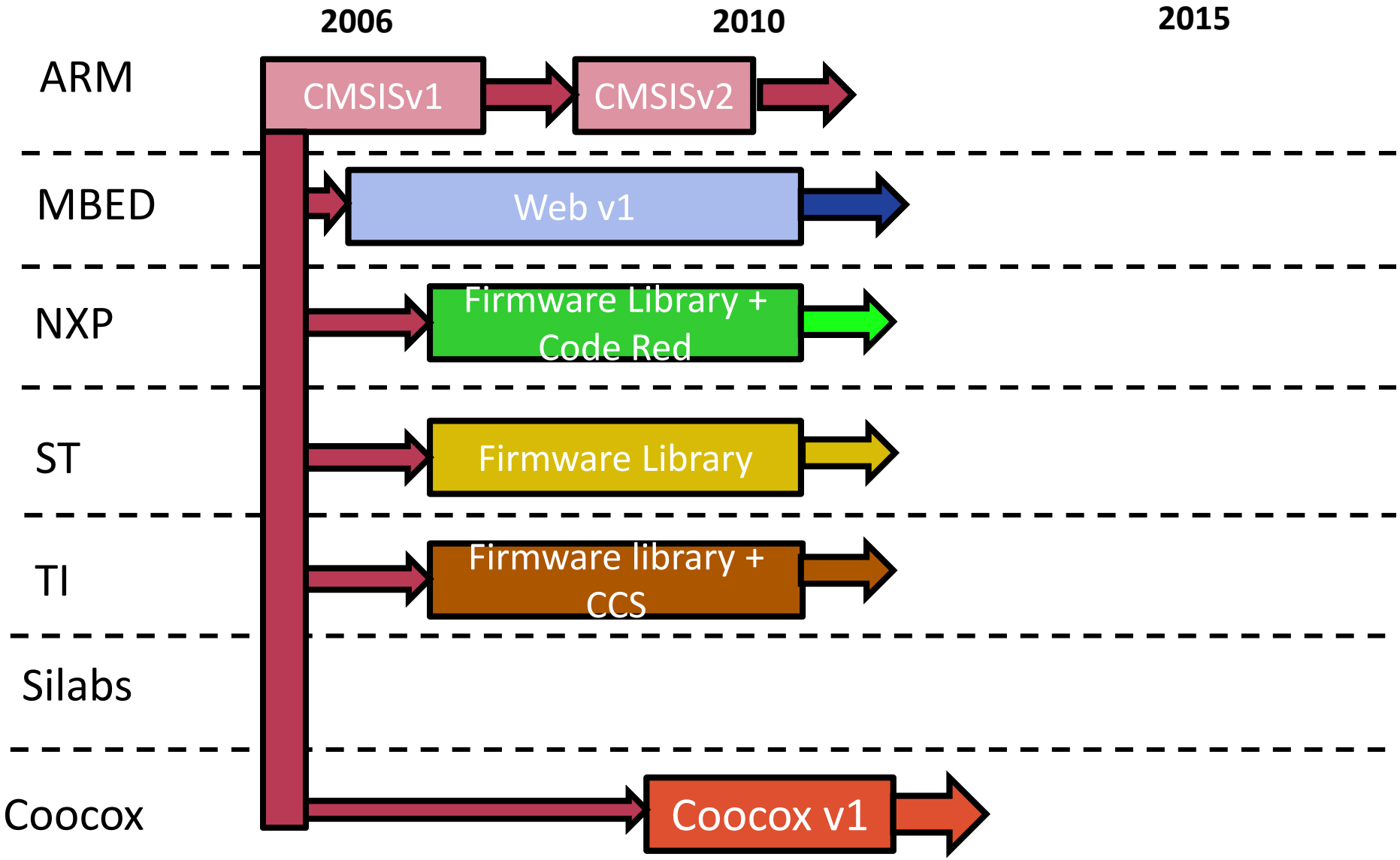
= recessive / dominant

A CAN controller



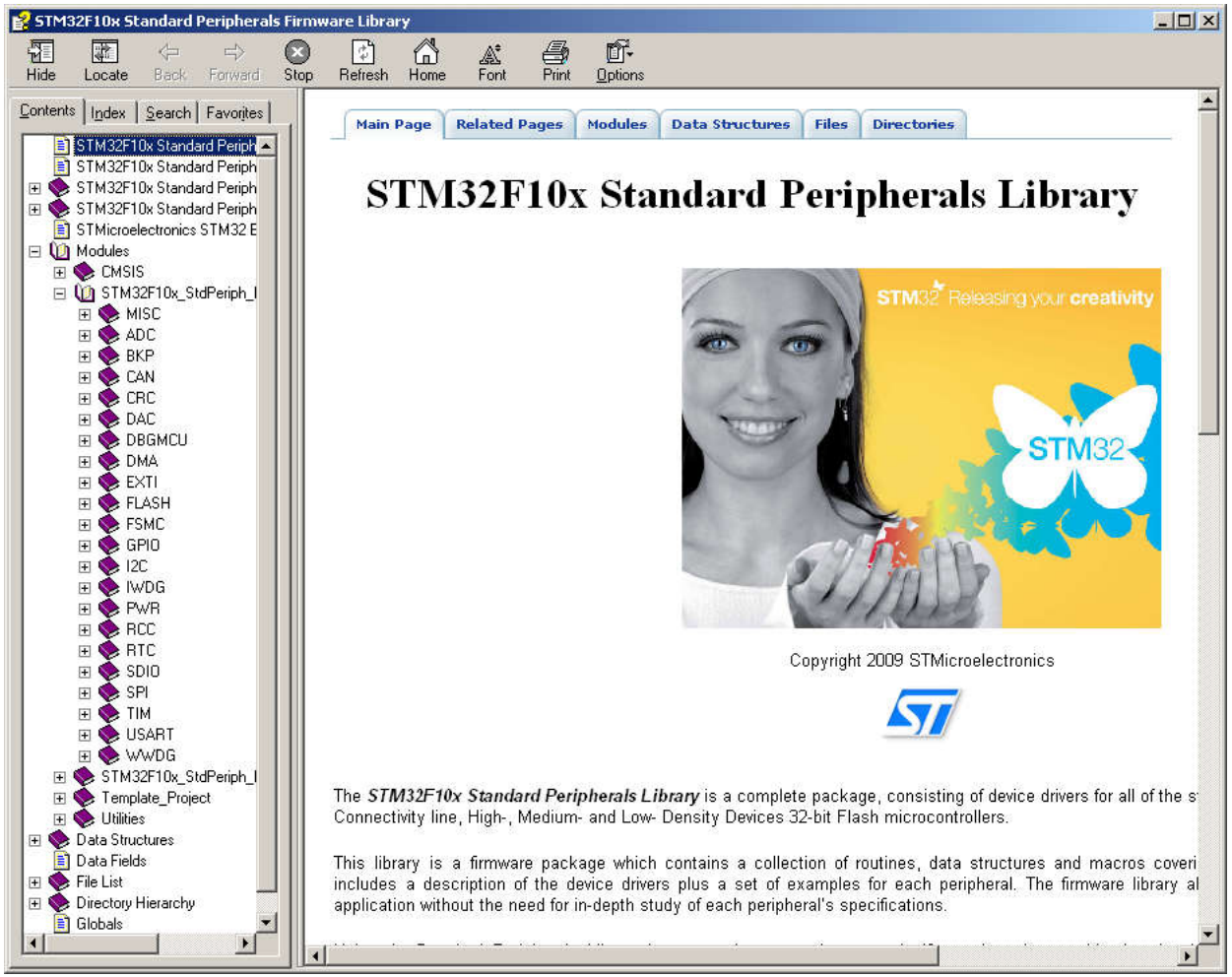
Firmware Librarys
~ 2010

Software support trends 2010



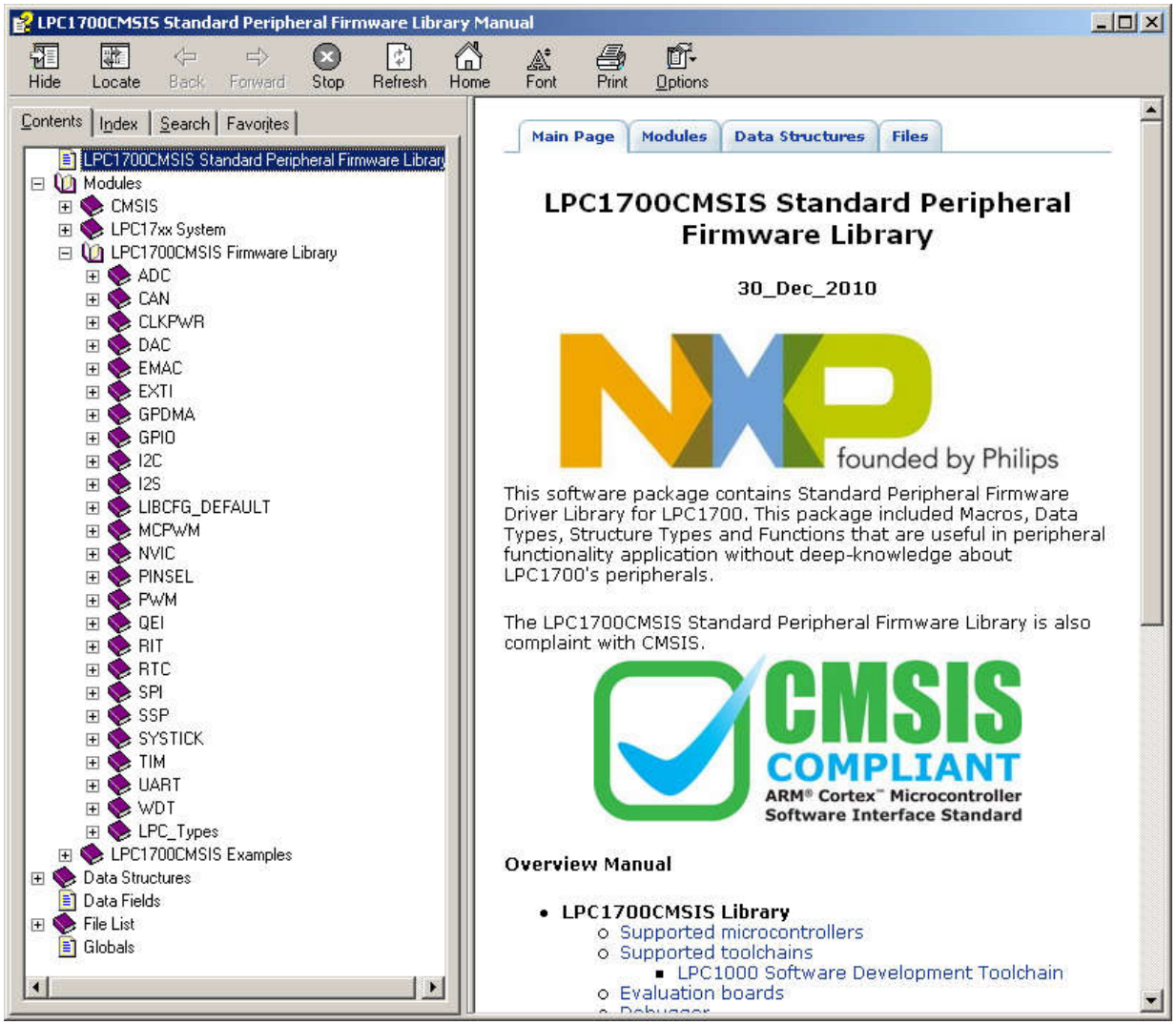
ST's old firmware library

- Commented in Doxygen
- Using Modules
- Many examples



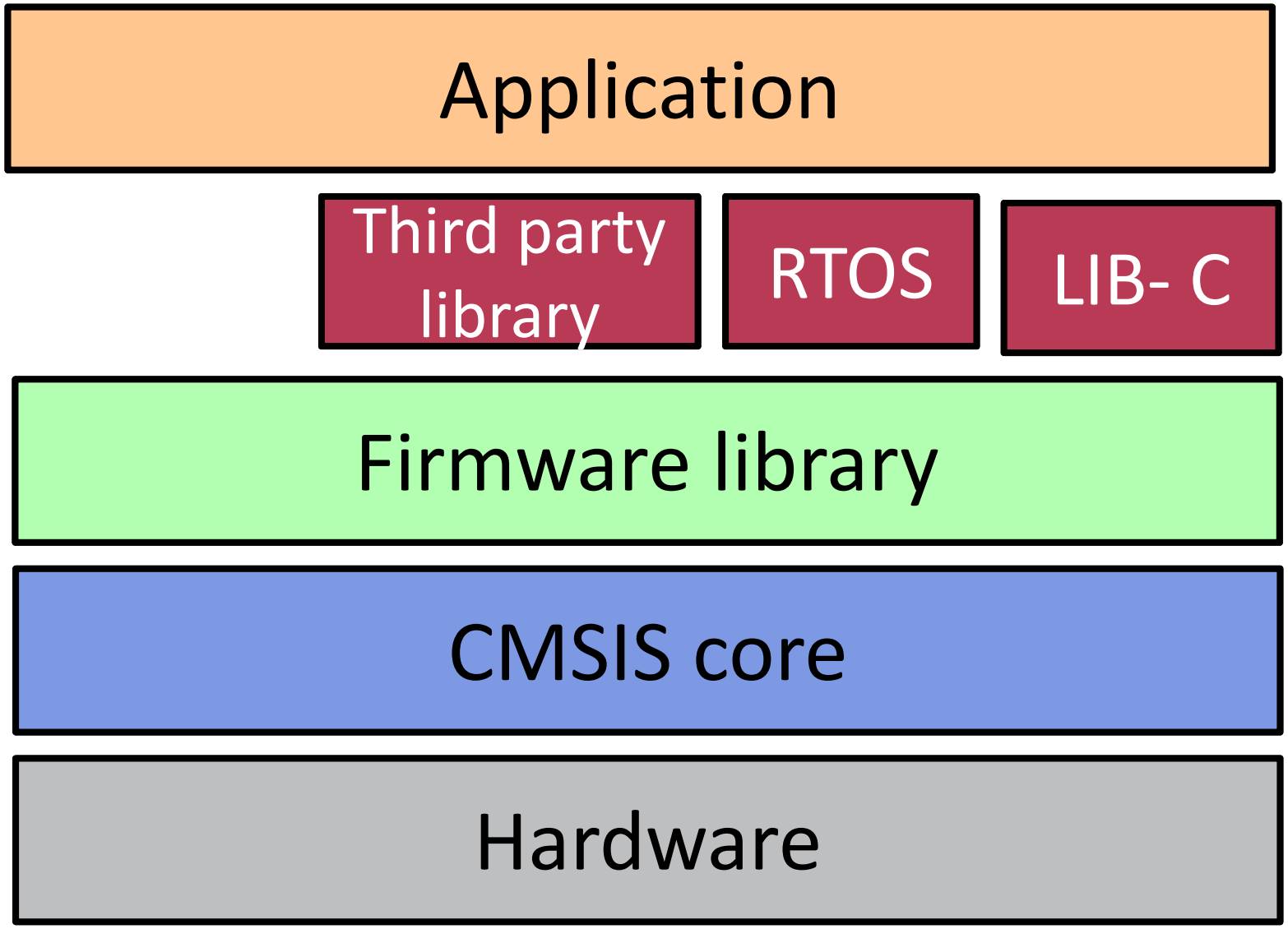
Firmware library of NXP

- Commented in Doxygen
- Using Modules
- Many examples



Software architecture
LIB-C

UART printf


Application
Third party library
RTOS
LIB- C
Firmware library
CMSIS core
Hardware

UART printf

- Syscall minimal porting
  - iprintf, printf differencies

```
60 __attribute__ ((used))
61 int _read(int file, char *ptr, int len)
62 {
63   return 0;
64 }
65 __attribute__ ((used))
66 int _write(int file, char *ptr, int len)
67 {
68   return len;
69 }
70
```