Laboratory Exercise 10

(Last updated: 14/02/2017, Tamás Krébesz)

Performance Evaluation of a 915-MHz FSK SoC Radio Transceiver

Required knowledge

- Digital communication schemes, especially frequency-shift-keying (FSK)
- Evaluation methods of digital communication schemes and transceivers
- Principle of digital frequency synthesis
- Operation principle of (super)heterodyne receiver
- Handling of microwave signal generator and spectrum analyzer
- Understanding the units used in microwave engineering (dBm, dB, dBc, …)

Objective

To give a deeper and application-oriented insight into the operation principle of an FSK transceiver that includes a complete transmitter and receiver implemented on a single chip. The TRF6900A Device Under Test (DUT) has been designed using the "System-On-a-Chip" (SoC) concept. It includes a simplex transceiver that operates in the 915-MHz Industrial, Scientific and Medical (ISM) frequency band. The (super)heterodyne receiver can receive both FSK and OOK signals.

The study of TRF6900A data sheets will help to understand the design concept of SoC integrated circuits, to learn the analysis and performance evaluation techniques of complex SoC ICs, to identify the main blocks of an FSK transceiver and to understand the operation principle of an FSK binary data communication system. The usage of microwave test equipment to be also learned and the application of the most frequently used microwave test configurations will be experienced. The students will study the application of FSK modulation scheme, they will measure the most important waveforms of an FSK transceiver and learn the basic principles of system-level measurements.

References

The following documents can be downloaded from the Webpage of the measurement:

-TRF6900A Eval Board User's Guide: 01_trf6900_user_manual_evaluation_board.pdf

-RF chip datasheet (trf6900A): 02_trf6900a_chip_data_sheet.pdf

03_trf6900a_how_to_design.pdf

-CERAFIL - Ceramic filters datasheet: 04_external_IF_filter_data_sheet.pdf

Test Equipment

Oscilloscope	Agilent 54622A
Spectrum Analyzer	Agilent E4411B ESA-L
RF Signal Generator with modulation capability	Agilent E4430B ESG-D
Power Supply	Agilent E3630
Function Generator	Agilent 33220A
Digital Multimeter (6½ digit)	Agilent 34401A

Help to understand readings (selections from Analog Devices engineering tutorials – see sourses for further details)

Phase-Locked-Loops (PLLs) (source: Analog Devices, MT-086 tutorial, Rev.0, 10/08)

FUNDAMENTAL PHASE LOCKED LOOP ARCHITECTURE

A phase-locked loop is a feedback system combining a voltage controlled oscillator (VCO) and a phase comparator so connected that the oscillator maintains a constant phase angle relative to a reference signal. Phase-locked loops can be used, for example, to generate stable output high frequency signals from a fixed low-frequency signal.

Figure 1A shows the basic model for a PLL. The PLL can be analyzed as a negative feedback system using Laplace Transform theory with a forward gain term, G(s), and a feedback term, H(s), as shown in Figure 1B. The usual equations for a negative feedback system apply.

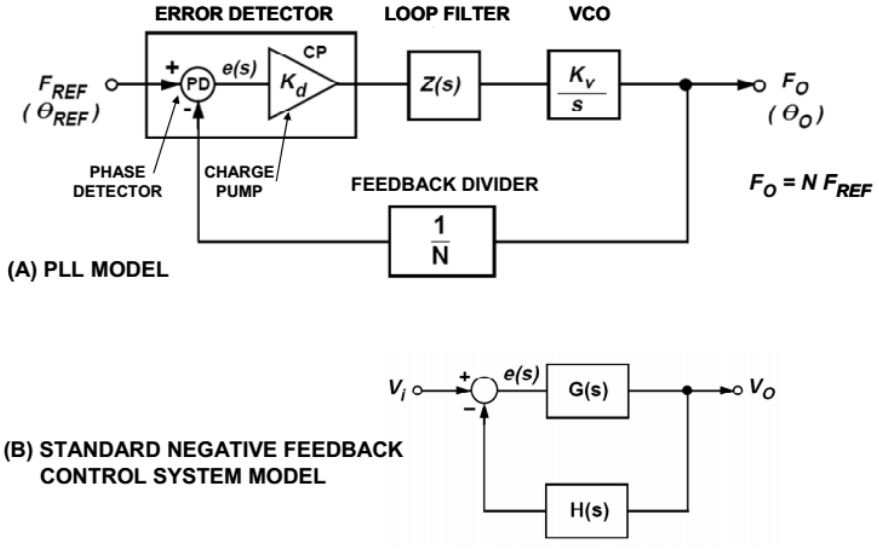

Figure 1: Basic Phase Locked Loop (PLL) Model

The basic blocks of the PLL are the *Error Detector* (composed of a *phase frequency detector* and a *charge pump*), *Loop Filter*, *VCO*, and a *Feedback Divider*. Negative feedback forces the error signal, e(s), to approach zero at which point the feedback divider output and the reference frequency are in phase and frequency lock, and $F_O = N_{FREF}$.

OSCILLATOR/PLL PHASE NOISE

A PLL is a type of oscillator, and in any oscillator design, frequency stability is of critical importance. We are interested in both long-term and short-term stability. Long-term frequency

stability is concerned with how the output signal varies over a long period of time (hours, days, or months). It is usually specified as the ratio, $\Delta f/f$ for a given period of time, expressed as a percentage or in dB.

Short-term stability, on the other hand, is concerned with variations that occur over a period of seconds or less. These variations can be random or periodic. A spectrum analyzer can be used to examine the short-term stability of a signal. Figure 5 shows a typical spectrum, with random and discrete frequency components causing a broad skirt and spurious peaks.

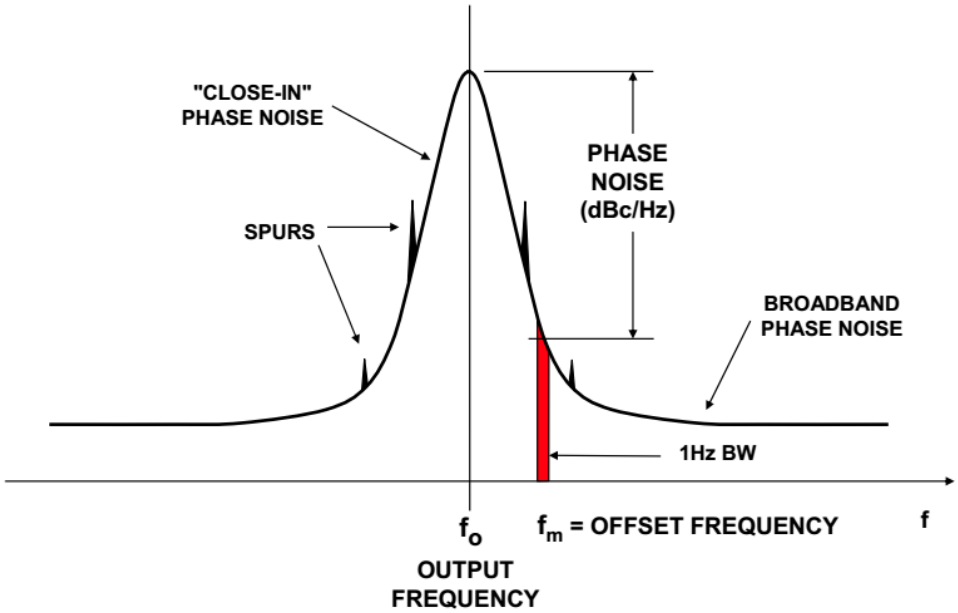

Figure 5: Oscillator Phase Noise and Spurs

The discrete spurious components could be caused by known clock frequencies in the signal source, power line interference, and mixer products. The broadening caused by random noise fluctuation is due to phase noise. It can be the result of thermal noise, shot noise, and/or flicker noise in active and passive devices.

The phase noise spectrum of an oscillator shows the noise power in a 1 Hz bandwidth as a function of frequency. Phase noise is defined as the ratio of the noise in a 1 Hz bandwidth at a specified frequency offset, fm, to the oscillator signal amplitude at frequency f_o.

Digital Frequency Synthesizer (DDS) and FSK (source: Analog Dialogue 38-08, August (2004))

How does a DDS device create a sine wave?

Here's a breakdown of the internal circuitry of a DDS device: its main components are a *phase accumulator*, a means of *phase-to-amplitude conversion* (often a sine look-up table), and a DAC. These blocks are represented in Figure 3.

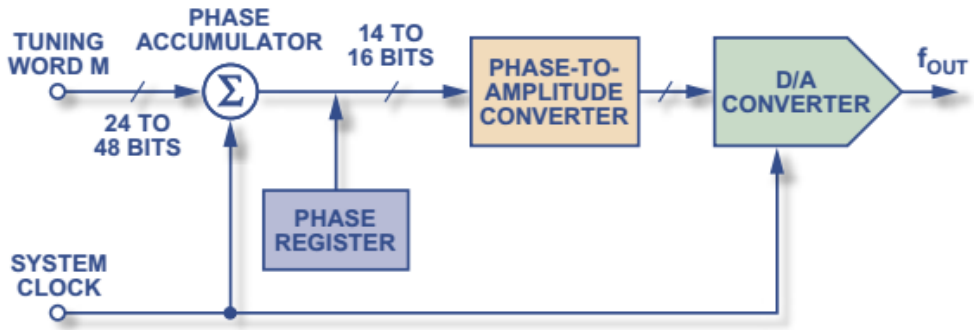

Figure 3. Components of a direct digital synthesizer.

A DDS produces a sine wave at a given frequency. The frequency depends on two variables, the *reference-clock* frequency and the binary number programmed into the frequency register (*tuning word*).

The binary number in the frequency register provides the main input to the phase accumulator. If a sine look-up table is used, the phase accumulator computes a phase (angle) address for the look-up table, which outputs the digital value of amplitude—corresponding to the sine of that phase angle—to the DAC. The DAC, in turn, converts that number to a corresponding value of analog voltage or current. To generate a fixed-frequency sine wave, a constant value (the phase increment—which is determined by the binary number) is added to the phase accumulator with each clock cycle. If the phase increment is large, the phase accumulator will step quickly through the sine look-up table and thus generate a high frequency sine wave. If the phase increment is small, the phase accumulator will take many more steps, accordingly generating a slower waveform.

How would I use a DDS device for FSK encoding?

Binary *frequency-shift keying* (usually referred to simply as FSK) is one of the simplest forms of data encoding. The data is transmitted by shifting the frequency of a continuous carrier to one of two discrete frequencies (hence *binary*). One frequency, f_1, (perhaps the higher) is designated as the mark frequency (binary one) and the other, f_0, as the *space* frequency (binary zero). Figure 6 shows an example of the relationship between the mark-space data and the transmitted signal.

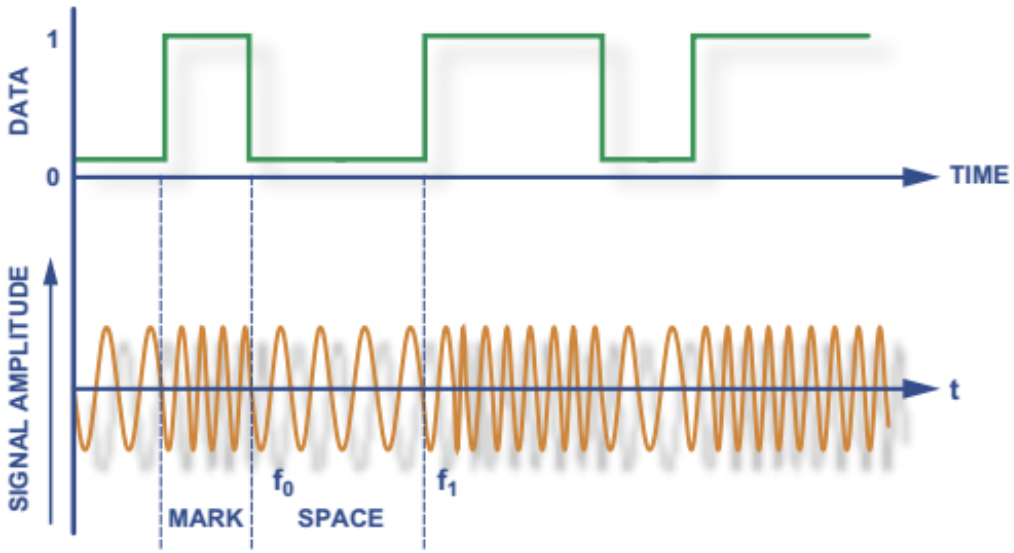

Figure 6. FSK modulation.

This encoding scheme is easily implemented using a DDS. The DDS frequency tuning word, representing the output frequencies, is set to the appropriate values to generate f_0 and f_1 as they occur in the pattern of 0s and 1s to be transmitted. The user programs the two required tuning words into the device before transmission.

Superheterodyne receivers and the mixer (source: Analog Devices, Basic Linear Design, Chapter 4 - RF/IF Circuits)

From cellular phones to 2-way pagers to wireless Internet access, the world is becoming more connected, even though wirelessly. No matter the technology, these devices are basically simple radio transceivers (transmitters and receivers). In the vast majority of cases the receivers and transmitters are a variation on the superheterodyne radio shown in Figure 4.1 for the receiver and Figure 4.2 for the transmitter.

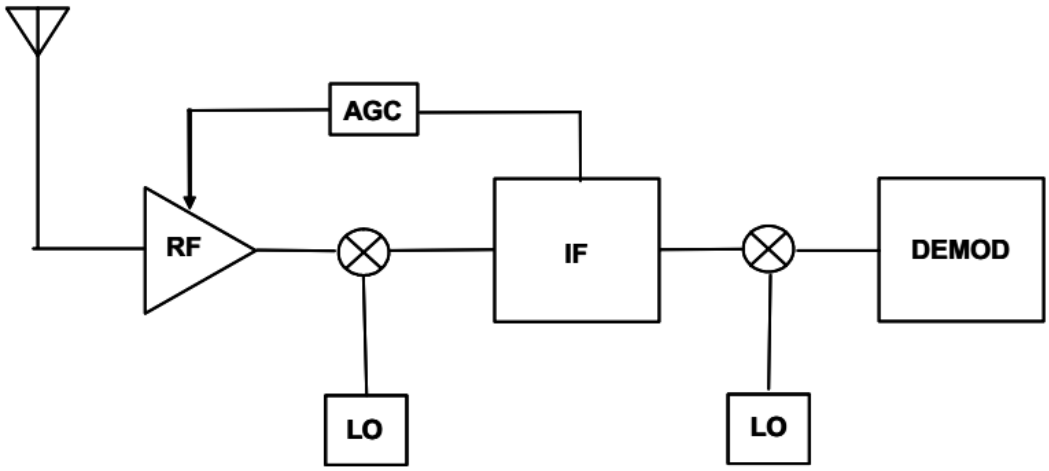

Figure 4.1: *Basic Superheterodyne Radio Receiver*

The basic concept of operation is as follows. For the receiver, the signal from the antenna is amplified in the radio frequency (RF) stage. The output of the RF stage is one input of a mixer. A Local Oscillator (LO) is the other input. The output of the mixer is at the Intermediate Frequency (IF). The concept here is that is much easier to build a high gain amplifier string at a narrow frequency band than it is to build a wideband, high gain amplifier. Also, the modulation bandwidth is typically very much smaller than the carrier frequency. A second mixer stage converts the signal to the baseband. The signal is then demodulated (demod). The modulation technique is independent from the receiver technology. The modulation scheme could be amplitude modulation (AM), frequency modulation (FM), phase modulation or some form of quadrature amplitude modulation (QAM), which is a combination of amplitude and phase modulation.

An idealized mixer is shown in Figure 4.3. An RF (or IF) mixer (not to be confused with video and audio mixers) is an active or passive device that converts a signal from one frequency to another. It can either modulate or demodulate a signal. It has three signal connections, which are called *ports* in the language of radio engineers. These three ports are the radio frequency (RF) input, the local oscillator (LO) input, and the intermediate frequency (IF) output.

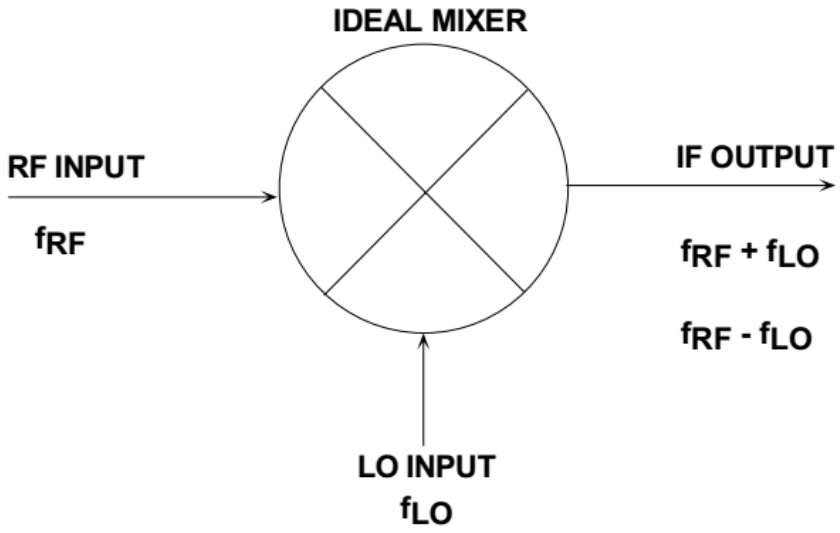

Figure 4.3: *The Mixing Process*

A mixer takes an RF input signal at a frequency f_{RF}, mixes it with a LO signal at a frequency f_{LO}, and produces an IF output signal that consists of the sum and difference frequencies, $f_{RF} \pm f_{LO}$. The user provides a bandpass filter that follows the mixer and selects the sum ($f_{RF} + f_{LO}$) or difference ($f_{RF} - f_{LO}$) frequency.

Evaluation board

In the conventional approach, different integrated circuits were devoted to the different signal processing tasks. To reduce the manufacturing cost, an up to date integrated circuit includes each signal processing circuit on a single chip, that is, an entire system is built on a single chip. This design approach is referred to as System-On-a-Chip (SoC) solution.

To make the application of complex SoC ICs easy to try for the costumers, evaluation modules (EVMs) are provided. Important inputs and outputs of the SoC IC are available for testing on the evaluation boards via SMA connectors. The parameters and operation modes of TRF6900A embedded into the EVM are controlled by the parallel port of a PC.

This laboratory exercise evaluates the performance of a 915-MHz FSK transceiver embedded in the TRF6900EVM evaluation module. See References for the preparing materials.

This description summarizes the operation principle of TRF6900A transceiver and explain the usage of TRF6900 evaluation board. To avoid confusion this description uses the terminology and notation introduced by the TRF6900A Data Sheets.

1. System level description and blocks of the TRF6900A transceiver

The TRF6900A SoC IC implements a low cost Frequency Shift Keying (FSK) transceiver that establishes a frequency-agile, half-duplex, bidirectional RF radio link. The device is available in a 48-lead TQFP package and is designed to provide a fully-functional multichannel FM transceiver. The transceiver is intended for digital FSK modulated applications in the 868-MHz European and in the North American 915-MHz ISM bands. The single chip transceiver operates down to 2.2 V and is expressly designed for low power consumption. The synthesizer has a typical channel spacing of approximately 230 Hz to allow narrow-band as well as wide-band applications. Even an inexpensive reference crystal can be used since its frequency error can be compensated by the narrow channel spacing of the Direct Digital Synthesizer (DDS). The DDS output is multiplied by a Phase-Locked Loop into the RF frequency band.
The European (868 MHz to 870 MHz) and North American unlicensed ISM frequency bands have been defined for short range devices with duty cycles from 0.1% to 100% in several sub-bands.
The building blocks of the TRF6900A transceiver are shown in Fig. 10-1 where the following main blocks can be identified:

- Direct Digital Synthesizer + PLL + Power Amplifier = Transmitter;
- LNA (Low-Noise Amplifier) + Direct Digital Synthesizer + PLL + RF Mixer + (filters and gains) + FSK Demosulator + Data slicer = Receiver
- Serial interface = reception of control words from control PC via TRF6900A.exe control software.

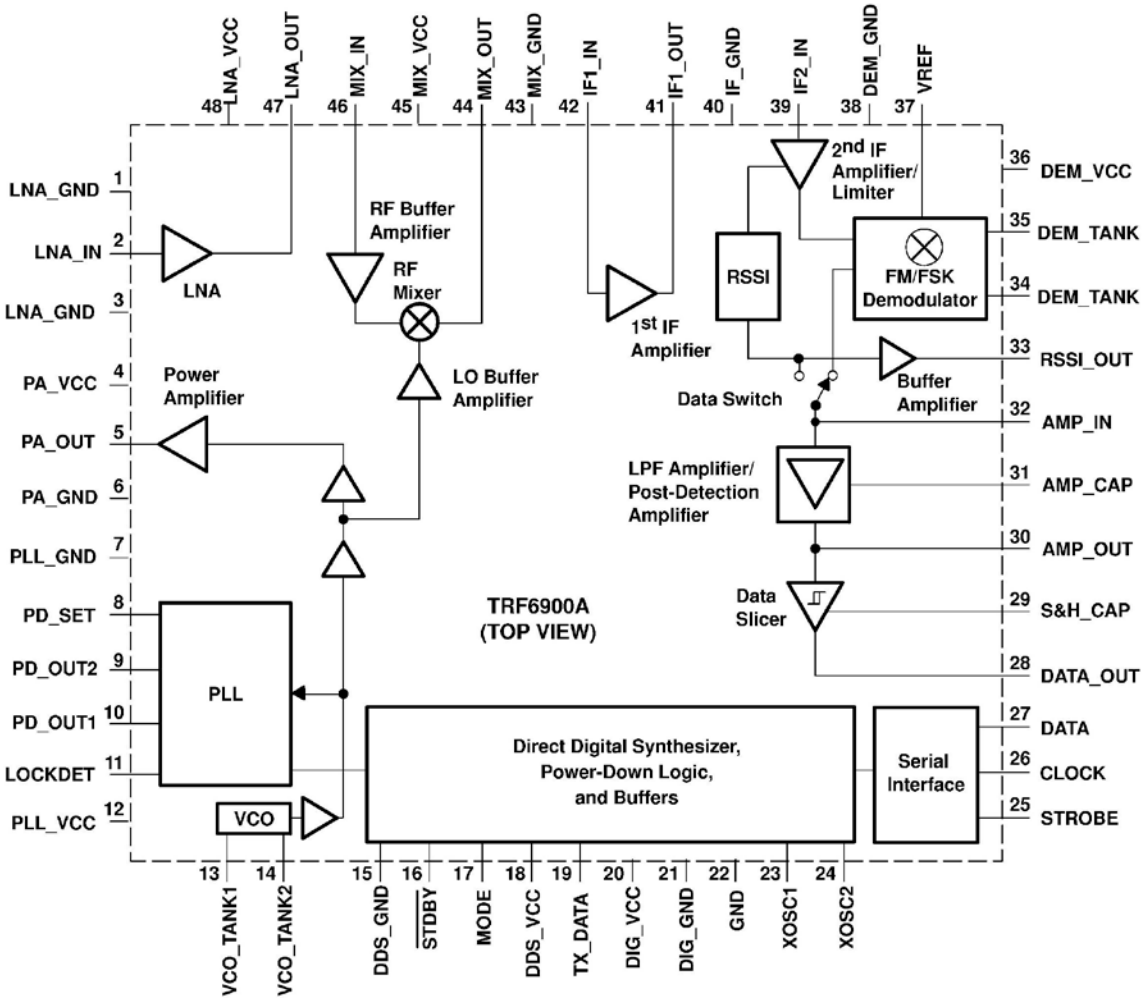

Fig. 10-1. Building blocks of the TRF6900A transceiver.

Direct Digital Synthesizer (frequency synthesizer) and FSK modulator

In transmit mode the frequency synthesizer performs two actions: it generates the RF input for the power amplifier and also operates as an FSK modulator. In receive mode the frequency synthesizer generates the unmodulated local signal for the mixer.

Transmitter

Since the output of frequency synthesizer is an FSK modulated RF signal where the synthesizer is tuned to the desired output frequency the transmitter contains only a multistage power amplifier as shown in Fig. 10-1.

The gain of power amplifier can be selected from three different values. Since the +4.5-dBm output power is enough for most of the applications, generally there is no need for an external power amplifier.

Receiver

TRF6900A IC contains a single-conversion heterodyne receiver with IF tunable between 10 MHz and 21.4 MHz. The local signal of the mixer is provided by the frequency synthesizer.

The gain of the low-noise amplifier (LNA) can be switched between two distinct values (2 dB and 13 dB) to compensate partly the variation in received signal level. In case of FSK modulation the received signal level typically varies between –101 dBm and –24 dBm. The frequency discriminator supports the reception of both digital FSK and analog FM signals. However, note that the transmitter can generate only FSK signals. The receiver contains a received signal strength indicator (RSSI) that has a linear characteristic over a wide range of received signal level. The signal level indicator also supports the reception of digital OOK modulation. The receiver is equipped with an Automatic Frequency Control (AFC) circuit that (i) tunes the frequency of the frequency discriminator to the center frequency of received signal and (ii) sets the decision threshold level of data slicer to its optimal value in digital communications.

Serial interface

The synthesizer frequency and the parameters of the TRF6900A transceiver can be set by 4 code words in two operation modes (Mode0 and Mode1). The serial interface, shown in Fig. 10-1, is used to enter the 4 serial code words into the IC registers. Two synthesizer frequencies can be pre-programmed in Mode0 and Mode1 and then the synthesizer frequency can be changed in an extremely short time between the two preprogrammed frequencies with a single command bit. Since there is no need for entering a new command word, this feature allows a very quick change between two reception frequencies or a quick change between reception and transmission.

Matching

To achieve the best noise performance and maximum power transfer, the blocks of the TRF6900A transceiver are matched to each other and to the antenna. The transmitter output and the receiver input are matched to 50 Ω. The terminations provided for the ceramic IF filters are 330 Ω.

2. Operation of TRF6900A transceiver and TRF6900 EVM

The TRF6900EVM evaluation board operates in the North-American 915-MHz ISM band. The typical application schematic of TRF6900A is shown in Fig. 10-2.

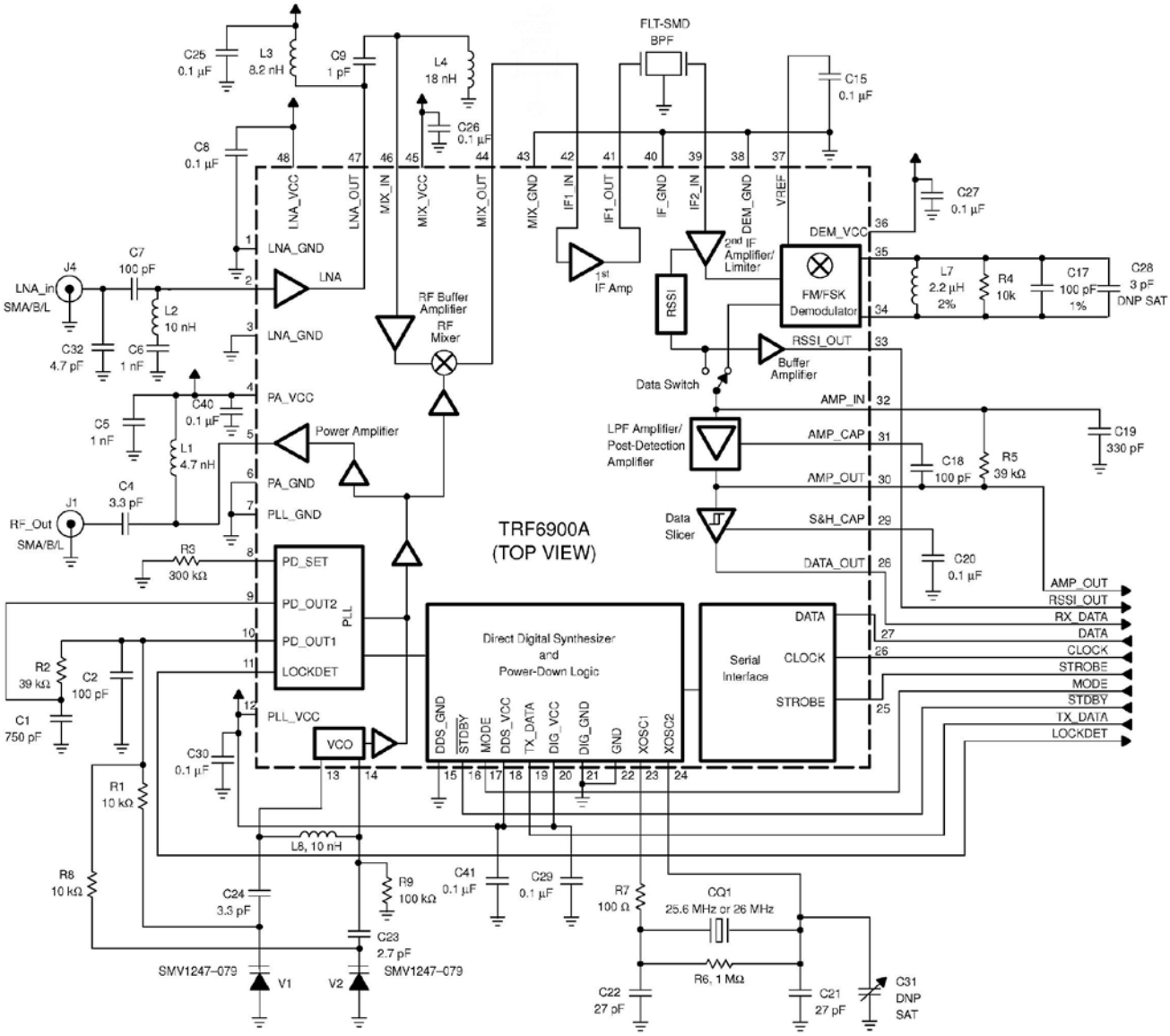

Fig. 10-2. Typical application schematics for the TRF6900A FSK transceiver. Note, one external IF channel (selection) filter is used, the IF frequency is 10.7 MHz.

Frequency synthesizer and FSK modulator

As shown in Fig. 10-3, the frequency synthesizer and FSK modulator block contains a direct digital synthesizer and a Charge Pump Phase-Locked Loop (CP-PLL). The frequency synthesizers used in transceivers are generally referred to as local oscillators or local oscillator blocks. The circuit elements being outside the dashed curve are not included in the chip but are added as external circuit elements. The building blocks of TRF6900A local oscillator are as follows:

Phase Frequency Detector	PFD
Charge Pump	CP

Loop Filter	
Varactor and LC Tank	
1/N Frequency Divider	
Oscillator (Voltage Controlled Oscillator)	VCO
Direct Digital Synthesizer	DDS
Digital Interface	
Xtal Oscillator	CLOCK
Clock, Data, Strobe input	

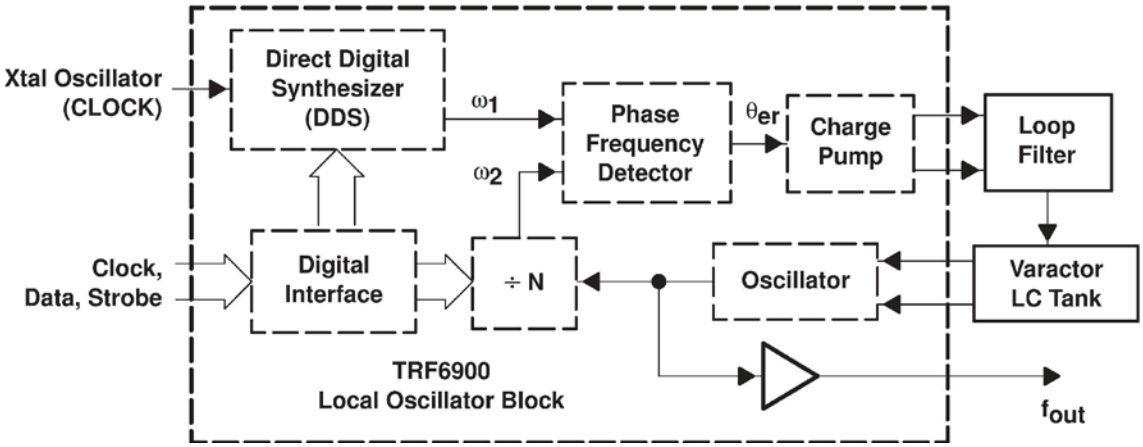

Fig. 10-3. Block diagram of the TRF6900A local oscillator.

The unmodulated carrier and the FSK modulated signal is generated by the DDS circuit. The DDS output frequency is about 3.5 MHz, this DDS frequency is multiplied to the ISM band by a charge-pump PLL circuit. The PLL multiplication factor is determined by the frequency divider placed in the feedback path of the PLL. The frequency division ratio denoted by N in Fig. 10-3 can be set to two values, 256 and 512.

In case of transmitting an FSK signal, the modulated signal has to get through the PLL without distortion. The distortion free transmission is achieved if the PLL closed-loop bandwidth is equal to K times of the signaling rate of modulation where $1.3 \leq K \leq 2.0$.

The Power Spectral Density (psd) of local noise is expressed as a function of the frequency detuning from the carrier frequency. The psd of the local noise can be optimized by the PLL closed-loop bandwidth.

If the frequency detuning from the carrier is less than the PLL closed-loop bandwidth then the psd of local noise is constant. The source of that noise is the DDS circuit, its output noise is amplified by a factor of N^2 where N is the frequency multiplication factor of the PLL. If the detuning exceeds the PLL closed-loop bandwidth then the psd of local noise is equal to the VCO noise that typically declines by –20 dB/D.

To shorten the frequency switching time, the closed-loop bandwidth of CP-PLL is increased during the frequency switching transient by adding extra current to the charge pump circuit. This extra current is provided by a second PFD marked by the PD_OUT2 in Fig. 10-2.

DDS circuit offers a very efficient solution to frequency synthesis, its benefits are as follow:

- extremely fast frequency and phase switching with preserving the phase continuity during the switching transient
- output frequency can be changed in tiny steps (high resolution in synthesized frequency)
- beyond the digital circuits, it needs only one analog low-pass filter to built

The applicability of direct digital synthesis is limited by the facts that

- only low frequency signal generation is supported as the output frequency must be less than one fourth of the clock frequency
- considerable amount of spurious signals appears in the output signal. Their level can be reduced by increasing the ratio of clock-to-output frequencies.

The block diagram of the DDS used in TRF6900A is shown in Fig. 10-4, where f_{CLK} is the clock frequency and f_{DDS} denotes the output frequency of the DDS. The output signal of the DDS is used as the reference signal of the PLL (see Fig. 10-3).

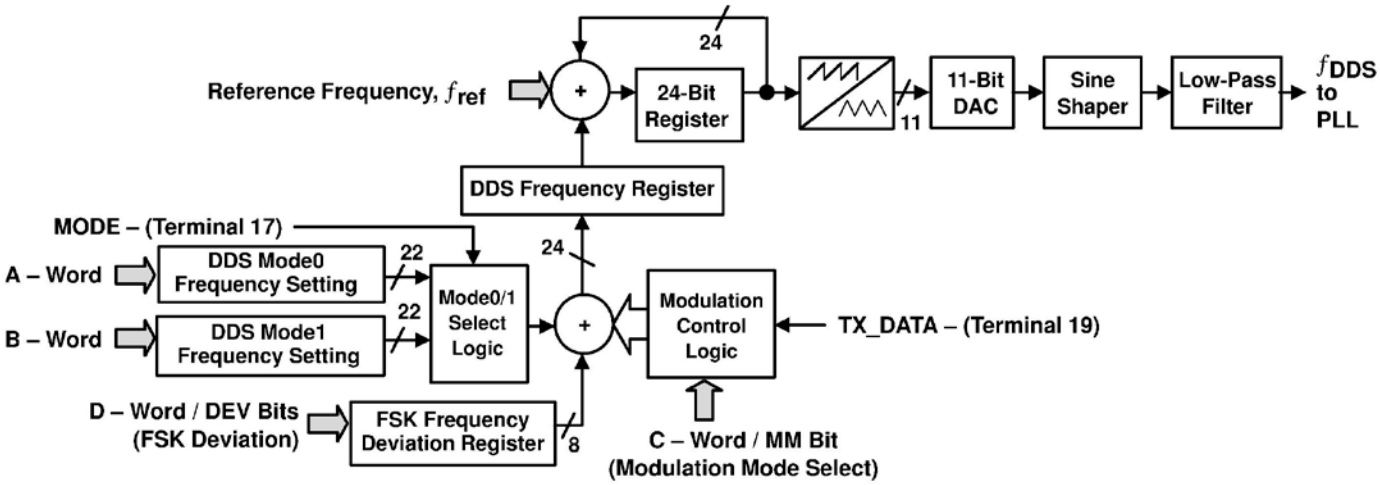

Fig. 10-4. Block diagram of the DDS used in TRF6900A.

The building blocks of DDS used in TRF6900A local oscillator are as follows:

Clock Frequency	f_{CLK}
24-Bit Register	
11-Bit DAC	DAC
Sine Shaper	
Low-Pass Filter	
to PLL	f_{DDS}

DDS Frequency Register	
Modulation Control Logic	
DDS Mode 0/1	DDS_x
Mode 0/1 Select Logic	
FSK Frequency Deviation Register	DEV

Figure 10-4 shows the operation principle of DDS used in TRF6900A. The content of the 24-bit register is increased at each clock tick by the number stored in the DDS frequency register until the 24-bit register overflows. Then counting cycle is restarted. The output of the 24-bit register equals to the instantaneous phase of the output signal, thus the digital signal looks like a sawtooth signal if it is plotted as a function of time.

The sawtooth signal is converted into a digital triangular one then the triangular signal is converted into an analog signal by means of a 11-bit Digital Analog Converter (DAC). The analog triangular signal is fed into a nonlinear circuit that converts the analog triangular signal into a sinusoidal one.

The output of the sine shaper is a staircase approximation of an ideal sinusoidal signal. Spurious signals appearing due to the staircase approximation are suppressed by an analog low-pass filter, the only analog component of DSS, characterized by a cutoff frequency of 4 MHz. This cutoff frequency limits the largest frequency that can be synthesized by the DDS.

The DDS output frequency f_{DDS} is determined by the number stored in the DDS Frequency Register. That number depends on three parameters:

- in case of Mode0 it is set by the code word „A,"
- in case of Mode1 it is set by the code word „B" and
- in case of FSK modulation it is influenced by code word „D" that determines the FSK deviation.

The very fast change of the output frequency of the DDS supported by A-Word and B-Word, the two frequency registers. Mode switch chooses the valid code word. The mode switch can be set by sending a MODE control signal to pin 17 of the IC. The value of output frequency is determined by code word "A" and code word "B" in case of operation mode "0" and "1", respectively.

Let the actual value of code words „A" and "B" be denoted by DDS_x. Assume that the synthesized signal does not carry an FSK modulation. Then the output frequency of the frequency synthesizer is given by

$$f_S = N f_{DDS} = N \frac{DDS\_x}{2^{24}} f_{CLK} = f_{S1:TX\_DATA=Low}$$

where N is the division ratio of the frequency divider used in the feedback path of PLL. The clock frequency f_{CLK} used in TRF6900EVM is 26.000 MHz.

One of the most important property of a frequency synthesizer is the minimum tunable difference between two adjacent output frequencies that is referred to as frequency raster or channel spacing

$$\Delta f_S = N \frac{f_{CLK}}{2^{24}}.$$

In case of FSK modulation the digital bit stream to be transmitted switches the DDS output frequency between two distinct values denoted by f_{S1} and f_{S2}. The digital bit stream has to be fed into the input TX_DATA (pin 19 of the IC). When the modulation input is low (bit „0") then the Modulation Control Logic has no effect on the DDS output frequency and it becomes identical with the unmodulated output frequency. Note, this operation principle of FSK modulator means that the transmit filter has to be modeled by a Zero-Order Hold (ZOH) circuit.

When high level (bit „1") is applied to the modulation input denoted by TX_DATA then the Modulation Control Logic adds the number DEV provided by the Code Word „D" to the content of the DDS frequency register. The output frequency of the frequency synthesizer is obtained as

$$f_{S2:TX\_DATA=High} = N\frac{DDS\_x + 4DEV}{2^{24}} f_{CLK}.$$

From equations above, the carrier frequency of the FSK modulated signal is obtained as

$$f_{FSK} = \frac{f_{S1:TX\_DATA=Low} + f_{S2:TX\_DATA=High}}{2}$$

and its deviation is

$$\Delta f_{FSK} = \frac{f_{S2:TX\_DATA=High} - f_{S1:TX\_DATA=Low}}{2} = N\frac{DEV}{2^{23}} f_{CLK}.$$

Transmitter

The TRF6900A transmitter contains only a three-stage power amplifier that is matched to the 50 Ω terminating impedance (see Fig. 10-2) by an LC circuit. The output power can be set to +4,5 dBm, −0,5 dBm and −8 dBm or the power amplifier can be switched off by the control bits found in code words „C" and „D".

Receiver

As shown in 10-2, the received signal is amplified by a low-noise pre-amplifier (NF=3,3 dB), whose gain can be set to 2 dB and 13 dB by the bits LNAm defined by the Code Words „C" and „D." The received signal is transposed into the IF band by a double balanced mixer, a Gilbert cell almost exclusively used in ICs to implement a mixer. Since the IF frequency is not high enough, an image filter cannot be used, therefore the sensitivity of the receiver is the same for the desired and the image signals.

The attenuation of ceramic filter (BW 150 kHz, denoted by BPF) is compensated by the IF pre-amplifier. The receiver selectivity is determined by the channel filter BPF.

The output of the channel filter is fed into an IF main amplifier that includes differential amplifiers offering 80-dB gain and a limiting capability. An important feature of digital FSK and analog FM modulations is that they can be processed by nonlinear receivers, therefore there is no need to apply linear amplifiers and AGC (Automatic Gain Control) circuits. The limiter needs approx. 32 μV at the input IF2_IN in order to provide limitation, that is, to fix signal level at the demodulator input.

The output signal of the limiter is fed into a frequency discriminator that supports the demodulation of both FSK and FM signals. The block diagram of quadrature-demodulator is shown in Fig. 10-5. The frequency discriminator converts the input FM into Phase Modulation (PM) and demodulates the PM by a multiplier followed by a low-pass filter.

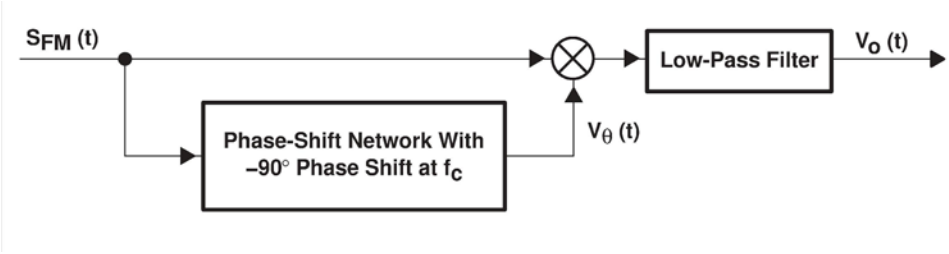

Fig. 10-5. The block diagram of frequency discriminator.

The frequency modulated $s_{FM}(t)$ signal is fed into a phase shifter implemented by an RLC circuit. Since the phase shift depends on the instantaneous frequency of incoming signal, the phase shifter converts the input FM into PM retaining the original FM modulation. The value of phase shift at the carrier frequency is –90°, that is, if the input signal does not carry any FM then the two multiplier inputs are orthogonal.

The quadrature demodulator multiplies the output signal $v_\theta(t)$ of the phase shifter with the input signal $s_{FM}(t)$. Since both multiplier inputs carries the same FM, the FM is cancelled and the modulating signal $v_o(t)$ is recovered from the PM. The low-pass filter suppresses the sum-frequency output of multiplier.

The output of frequency discriminator is passed by a second order low-pass receive filter. The cutoff frequency of receive filter implemented on the TRF6900 evaluation module is 45 kHz. The demodulated analog FM modulation can be recovered or the eye diagram may be observed at the output AMP-OUT.

If a digital FSK signal is to be received then the AMP_OUT is fed into the Data Slicer. Clock recovery circuit is not used by TRF6900A, instead the demodulated bit stream is generated from the output of receive filter by a level comparator referred to as data slicer. The demodulated bit stream appears at the output of data slicer referred to as DATA_OUT.

The received signal strength indicator provides a DC voltage at RSSI_OUT that is linearly proportional to the power level of IF signal appearing at the input of IF main amplifier and limiter. Since the blocks preceding the IF main amplifier are linear, the RSSI_OUT voltage is linearly proportional to the received signal level, its sensitivity is 19mV/dB. The main task of the RSSI is to measure the power level of the received signal.

Because of its short response time (delay 1 μs) RSSI circuit can be applied to demodulate digital ASK and OOK signals. If signals carrying amplitude modulation are received then the input of low-pass receive filter has to be connected to the RSSI output via the data switch. The demodulated ASK and OOK signals appear at the DATA_OUT output of the data slicer.

Bit error rate of an FSK receiver and the distortion of an FM receiver depend strongly on the difference of the carrier frequency of received signal and the center frequency of the frequency discriminator. The threshold level of the decision circuit is another parameter that has a strong influence on the quality of the reception of digital modulations.

To cancel the distortions resulting from the frequency error and wrong decision threshold the TRF6900A has a special operational mode, referred to as learning mode. In learning mode a 010101... bit sequence is transmitted and the receiver is set to the learning mode by the SLCTL bit of Code Word „C.” In learning mode an AFC circuit cancels the frequency error by tuning the center frequency of the frequency discriminator to the carrier of received

signal and in case of reception of a digital modulation it optimizes the decision threshold level of the data slicer.

During the reception of an arbitrary data sequence, the receiver has to be set to the hold mode by the SLCTL bit of Code Word „C." In his hold mode, the receiver stores the center frequency of the frequency discriminator and the value of the optimum threshold level of data slicer.

The receiver should be operated continuously in learning mode when analog FM signals are received. However, in case of digital and/or burst communications the receiver must operate in hold mode and the training mode has to be switched on only regularly to cancel the frequency error and to optimize the decision threshold. Note, when the receiver operates in learning mode then the transmitter providing the signal to be received must transmit a special training sequence.

Serial interface

TRF6900A IC is controlled 4 code words depicted in Fig. 10-6. The definition of each bit of the control worlds can be found in the data sheet of TRF6900A transceiver (02_trf6900a_chip_data_sheet.pdf), refer to pages 24-26. The uploading sequence of entering the code words into TRF6900A is shown on the page 28 of the data sheets.

The DDS frequencies in mode „0" and mode „1" are assigned by code words „A" and „B," respectively. The blocks of TRF6900A can controlled be by bits 0-12 of code word „D" in mode „0" and by bits 0-12 of code word „C" in mode „1".

The parameters of the PLL and the state of the data switch are controlled by bits 15-20 of code word "C."

Deviation of FSK modulation can be set by bits 13-20 of code word "D."

The first bits (ADDR bits) of each code word carry the addresses of the four registers contained in the serial interface.

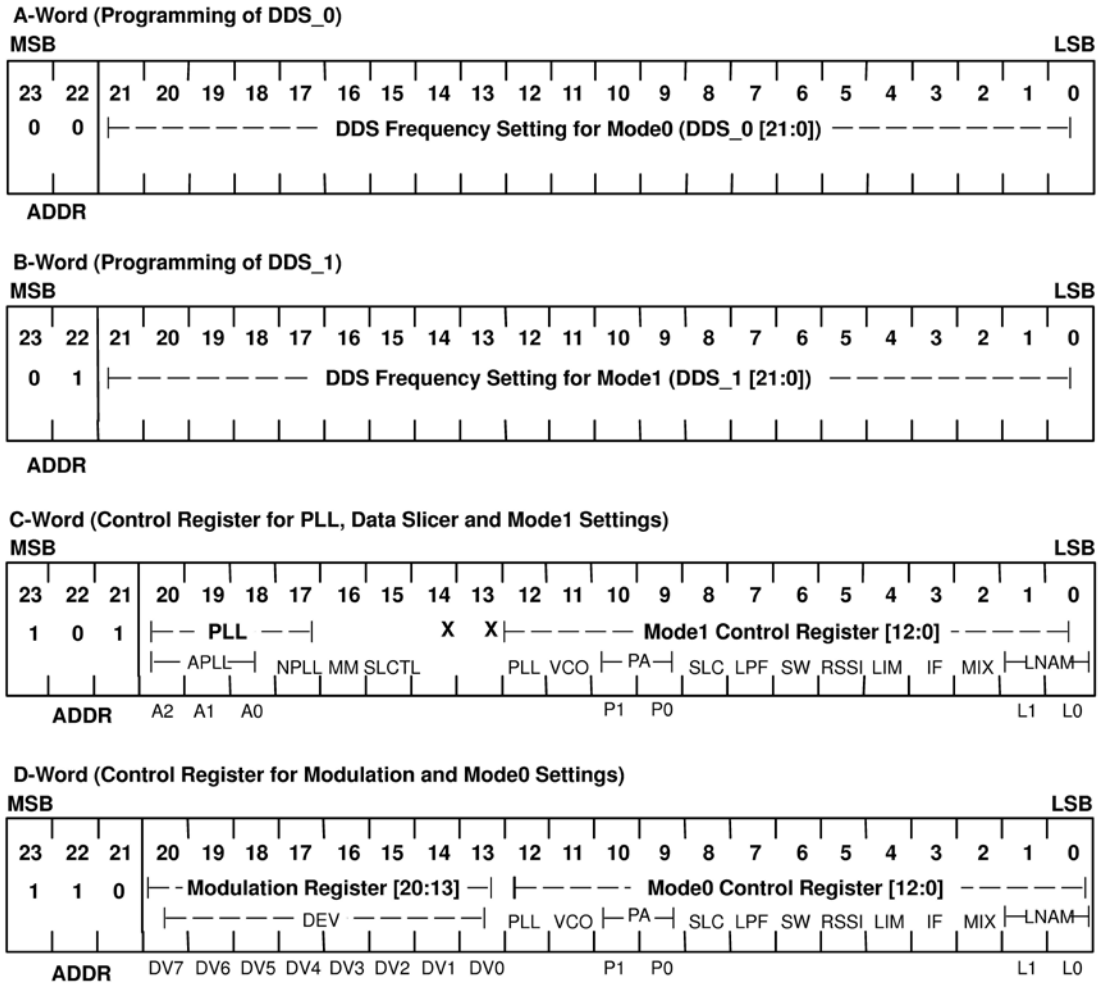

Fig. 10-6. Format of code words used to control TRF6900A integrated circuit.

3. Use of TRF6900EVM evaluation module and its software

TRF6900EVM evaluation module

As shown in Fig. 10-2, the TRF6900 evaluation module contains the TRF6900A transceiver circuit operating in the North American ISM band (902-928 MHz), the power supply unit and digital circuits required to upload the code words into the integrated circuit. The evaluation board can be connected to the parallel port of the host PC and testing of the TRF6900A IC can be achieved by a Windows-based software application accompanies the evaluation board.

The evaluation module supports a full test of TRF6900A. Different measurements can be achieved by changing the jumper positions and via the PC software. This manual refers to all the knowledge necessary for the successful completion of the laboratory experiment. All required jumper settings are shown in Fig. 10-7. The notations used on the TRF6900 evaluation module and in Fig. 10-2 are identical.

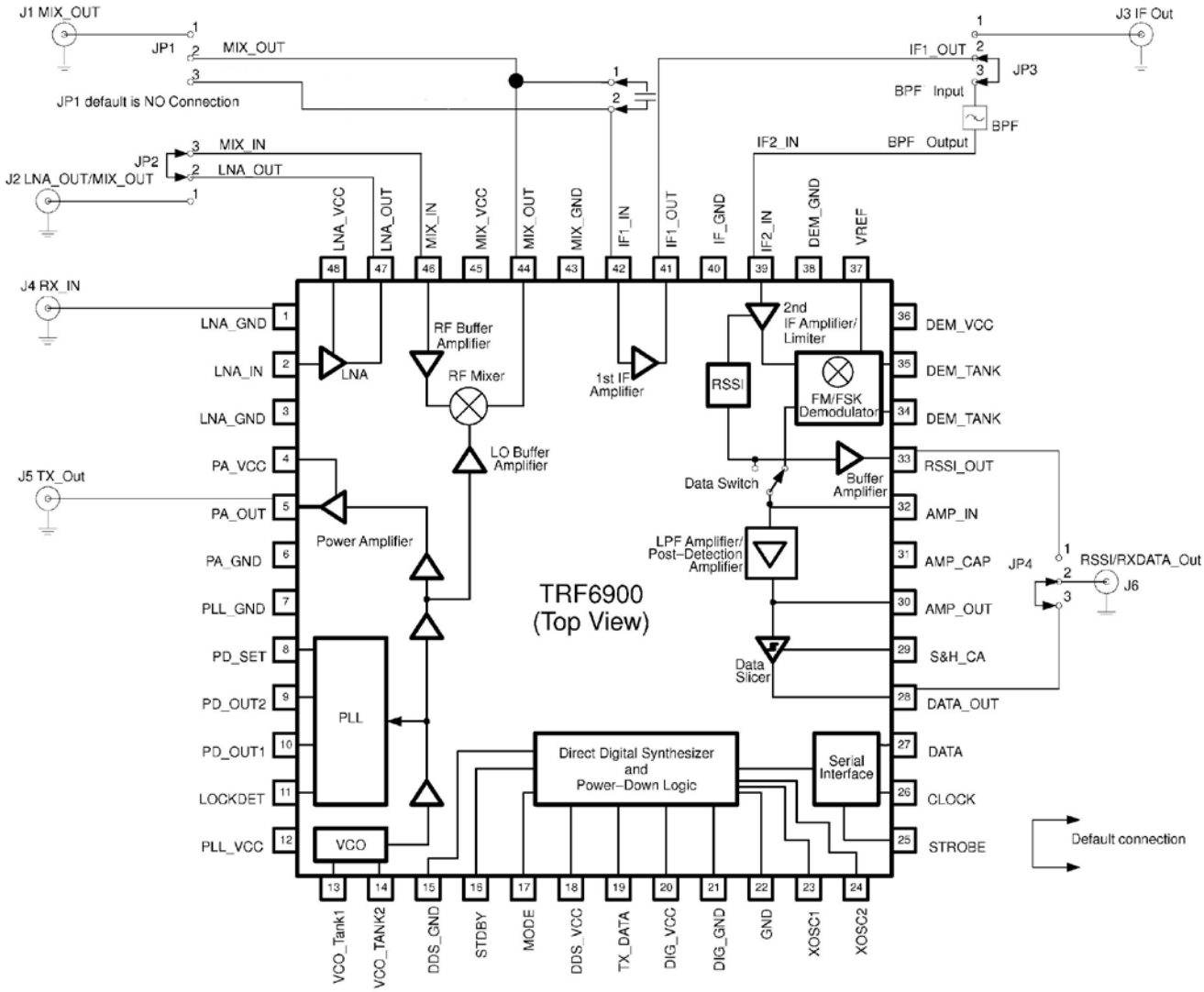

Fig. 10-7. Location of jumpers on the evaluation board

The following Test Points (TPs) and connectors, are available in he evaluation module, will be used during the laboratory experiment:

Connectors:

P1: not shown in Fig. 10-7

Terminal P1 have to be connected to the parallel port of the PC. The TRF6900 software controls TRF6900EVM evaluation board via terminal P1.

J4: RX_IN

SMA female connector that the input of the receiver is connected to.

J5: TX_OUT

SMA female connector that the output of the transmitter is connected to.

J6: RXDATA_OUT

SMA female connector that provides the demodulated digital bit stream.

Test points:

AMP_OUT (30th pin of IC)

Output of the low-pass receive filter placed after the demodulator. If analog modulation is received then this output provides the demodulated signal.

RSSI_OUT

Output of the received signal strength indicator circuit.

TXDATA

TXDATA has two tasks. If FSK signal with internal modulation is transmitted this output is used to monitor the transmitted bits stream.

When an external digital modulating signal is applied then the external generator has to be connected to this input. Note, **TXData must be switched off on the Main Program Screen when external modulation is applied!**

Led indicators: (not shown in Fig. 10-7):

VCC

VCC LED is on if power supply is on.

LDET

LDET LED is on if the PLL is locked.

ENABLE

ENABLE LED is on if STBY signal sent by PC is high.

Using TRF6900 software

TRF6900EVM evaluation board can be controlled via three windows:

Main Program Screen
Chip Layout Screen
PLL/Modulation Options Screen

In the followings the most important information on the control windows are collected. Only those parameters that are necessary for the successful completion of the measurement are considered. For further details please refer to 01_trf6900_user_manual_evaluation_board.pdf

Main Program Screen

Sections of the Main Program Screen shown in Fig. 10-8 are as follows:

SYNTHESIZER
From the DDS clock frequency, the PreScaler value (PLL multiplication constant) and the Desired Freq. of the frequency synthesizer the program calculates code words “A” and “B.”

As the frequency synthesizer is capable to generate frequencies only with discrete resolution, the actual frequency is shown in the Actual Freq. box.

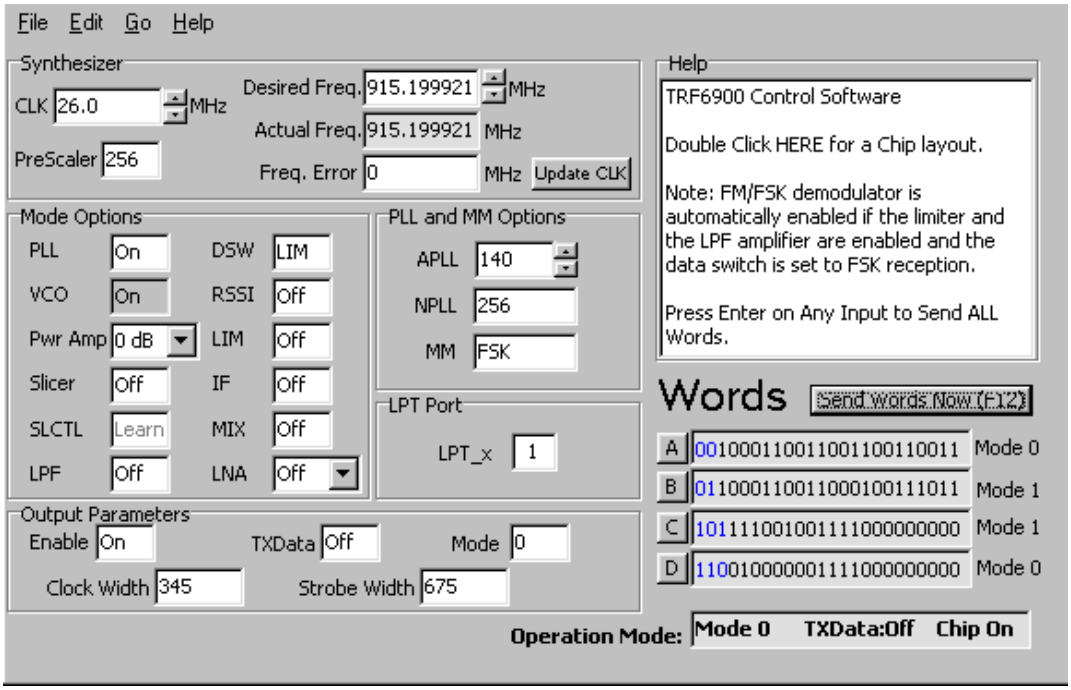

Fig. 10-8. Main program screen of the TRF6900 software.

Due to the imperfection of quartz crystal used to determine the clock frequency, the actual clock frequency differs from the desired value, that is, a frequency error exists. Consequently, the local frequency generated by the frequency synthesizer differs from Actual Freq. The procedure required to correct this frequency error using the Freq. Error and Update CLK boxes is discussed at the end of this chapter.

MODE OPTIONS

Boxes identified by the following abbreviations are used to switch on/off a certain circuit of the transceiver: PLL (phase locked loop), VCO (voltage controlled oscillator), Slice (decision circuit), LPF (low-pass filter), RSSI (received signal strength indicator), LIM (IF main amplifier and limiter), IF (IF pre amplifier), MIX (mixer) and LNA (RF low noise preamplifier).

Bow marked by Pwr Amp sets the output RF power level or it switches the power amplifier off. If the decision circuit is switched on then the learn/hold modes can be selected in the box SLCTL. Data switch is controlled via the box DSW.

OUTPUT PARAMETERS

The box Enable switches the state of TRF6900A transceiver on/off. When FSK signal is transmitted then the modulation can be altered manually between “0” and “1” via the box TXData . **In case of external FSK modulation**, that is, when an external bit stream is applied to the TXDATA test point from a square wave generator **then TXData must be turned off**. TRF6900A transceiver is suggested to operate always in Mode 0 during the laboratory experiment.

The other boxes are irrelevant and should not be changed during the laboratory experiment.

LPT PORT

PC controls the evaluation board via parallel port 1 by setting the box LPT_x = 1.

PLL AND MM OPTIONS

Box APLL increases the closed-loop bandwidth of PLL during acquisition. The larger the number the higher the current in the charge pump circuit and, consequently, the larger the bandwidth during acquisition. After locking, the extra charge pump current is set to zero. Box NPLL determines the frequency multiplication factor of the PLL. Box MM should be set FSK, to the only valid parameter.

WORDS

In boxes Words "A"-"D" the code words depicted in Fig. 10-6 are shown. Bits of the code words are calculated by the TRF6900 software but they are not valid until they are entered by pushing the button Send Words Now. The new bits already calculated but not uploaded yet are shown in red. Pushing the button Send Words Now all the bits are uploaded into the registers of TRF6900A transceiver, the new bits become valid and the bits in the box Words turns black.

USING THE MAIN WINDOW

Parameters can be set by double clicking on the left mouse button or by clicking on the arrows on the right hand side of the boxes. Clicking inside the help window makes Chip layout screen appear.

Chip Layout Screen

The Chip Layout Screen shows the block diagram of TRF6900A transceiver as depicted in Fig. 10-9. Clicking on a block changes the state or parameter of a circuit. The buttons Mode 0, TXData, Enable and Send Words have the same functions as the boxes with the same names provided on the Main Program Screen.

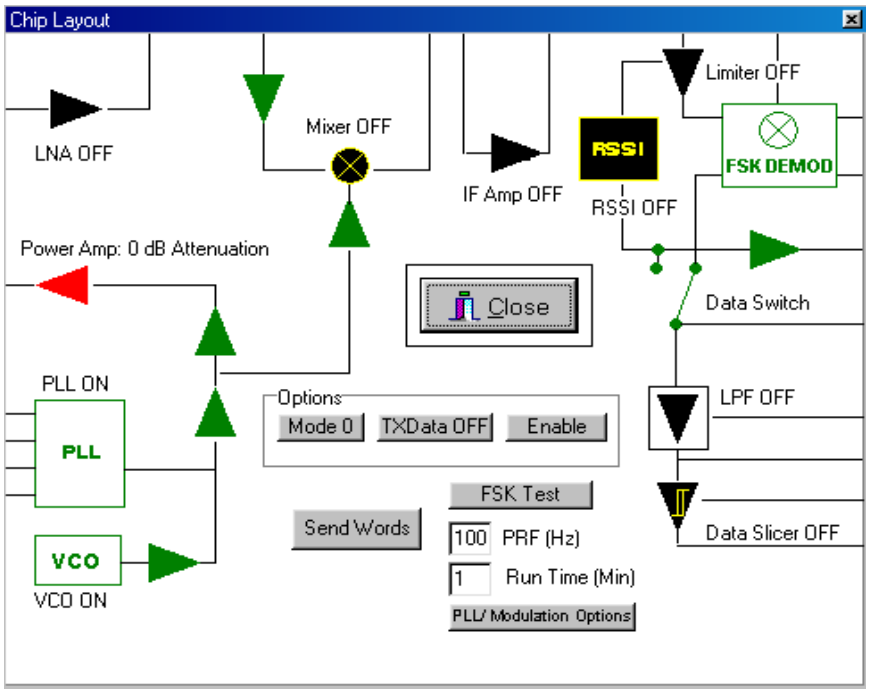

Fig. 10-9. Chip layout screen of TRF6900 software.

An FSK modulated waveform with an alternating “0”-“1” bit stream and 200-bit/s data rate is transmitted by clicking on button FSK Test. The time duration of FSK signal generation can be entered in minutes via the Run Time box.

The parameters of FSK modulation can be entered in a popup window. It appears after left clicking on the button of PLL/Modulation Options.

PLL/Modulation Option

As shown in Fig. 10.10, the left hand side of PLL/Modulation Option screen can be used for uploading the PLL parameters of the PLL. Note, these parameters can be also uploaded via the Main Program Screen.

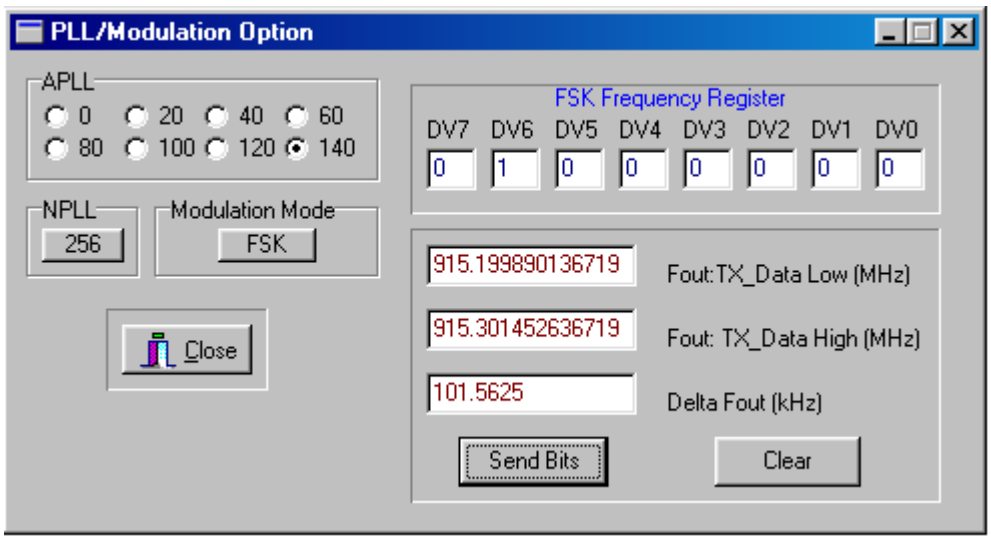

Fig. 10-10. PLL/Modulation Option Screen of the TRF6900 software.

The DEV number that determines the deviation of FSK modulation can be set by double clicking on boxes denoted by DV0—DV7. First the bits DV0—DV7 have to be set then these bits have to be entered into the TRF6900 software by clicking on the button Send Bits. The TRF6900 software calculates and shows the parameters of FSK modulation in the three boxes being below the DV0-DV7 ones. Be careful, Delta Fout shows the difference between the two FSK frequencies that is equal twice the FSK deviation. Parameters of FSK modulation are uploaded into the registers of TRF6900A transceiver only if the button Send Words Now on the Main Program Screen is pushed.

Correction of clock frequency error

Because of the imperfections of the quartz crystal used in clock oscillator, the actual clock frequency may differ from the value entered in the Main Program Screen. This error causes an error in the synthesizer frequency. The TRF6900 software corrects this error by searching for a synthesizer frequency being closest to the desired synthesizer frequency.

Steps of frequency error correction are as follows:

1. Enter the desired frequency in the Main Program screen, for example, enter 915.199921 MHz in the box of Desired Freq.

2. Measure the actual output frequency of the frequency synthesizer by an accurate frequency counter.
3. Enter the frequency difference being between the Desired Freq. and the measured one into Freq. Error box in MHz. Mind the sign!
4. The TRF6900 software will perform the necessary correction. Enter the corrected value of clock frequency by clicking on Update CLK button.

4. Test panel

TRF6900 Evaluation Module is embedded into test set shown in Fig. 10-11. To avoid overloading, 30-dB and 20-dB attenuators have been attached to the RX_IN input and to the TX_OUT output of the transceiver. Note, in the description of laboratory experiment the power levels measured at the inputs/outputs of the TRF6900 evaluation board are given. When setting and calculating the power levels the effect of the 30-dB and 20-dB attenuators has to be considered.

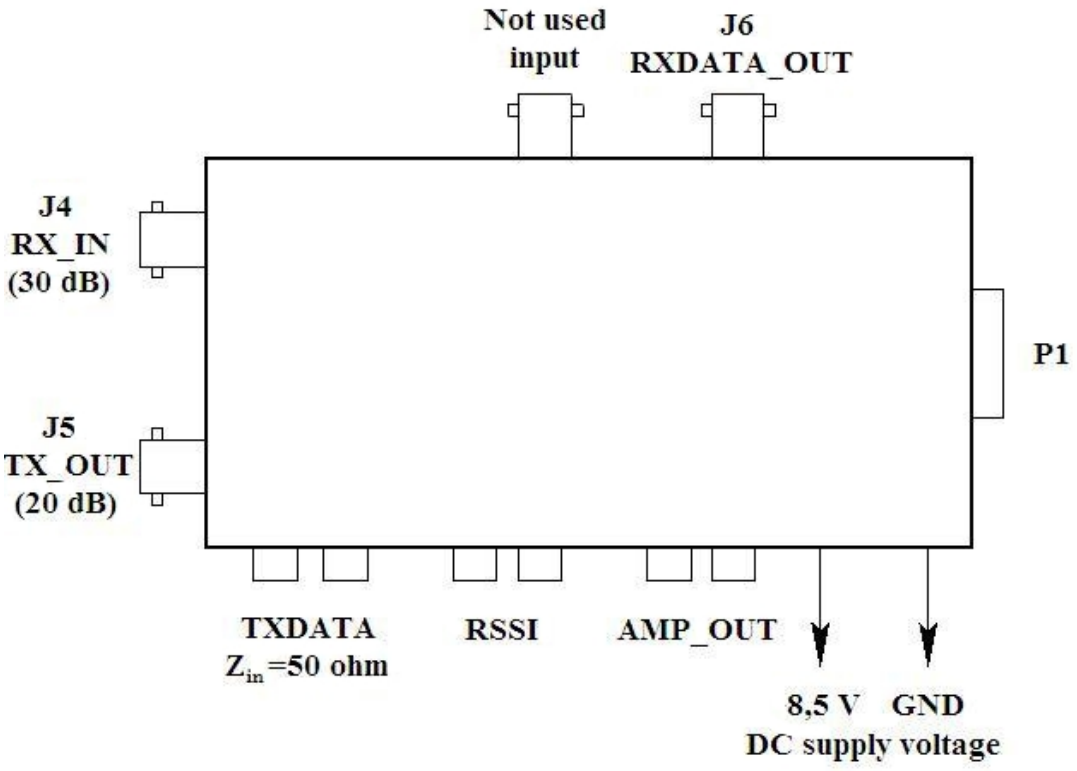

Fig. 10-11. Test set containing TRF6900EVM.

List of inputs and outputs can be found on test panel and used during measurement:

Power supply voltage: +8,5 V (max. input current = 200 mA).

RX_IN (J4, 30 dB)

Receiver input, available via a 30-dB attenuator.

TX_OUT (J5, 20 dB)

Transmitter output, terminated by a 20-dB.

RXDATA_OUT (J6)

Output of the decision circuit.

P1

Control input, it has to be connected to the parallel port of the PC.

TX_DATA (Z_{in}=50 Ω)

Input for external FSK modulation. Input impedance is 50 Ω!

RSSI_OUT

Output of received signal strength indicator. To be terminated by a high impedance.

AMP_OUT

Output of the low-pass receive filter following the demodulator.

Test questions

1. Sketch the block diagram of a PLL and highlight the VCO in it. What is the operation principle of a VCO?
2. Draw the block diagram of a PLL! What can we use a PLL for?
3. How can we decide that a receiver works well if we have the eye-diagram of the receiver plotted? Draw an eye-diagram and briefly explain it!
4. What do these letter words stand for: ASK, OOK, FSK, dBm, dBc?
5. In an FSK modulation system the frequency for bit „0” is 915,2 MHz. The frequency for bit „1” is 915,3 MHz. What is the value of the deviation?
6. The deviation of an FSK modulation is 250 kHz. The frequency for bit „0” is 1850 MHz. What can the frequency be for bit „1”?
7. The sensitivity of a receiver is -105 dBm. The transmitter radiates the information with -40 dBm. The attennuation of the channel is 80 dB. Is it possible to recover the information radiated?
8. What sensitivity should the receiver have if the information to be recovered is radiated by a transmitter with power level -50 dBm and attennuated by 70 dB travelling through the channel?
9. Some important parameters of a spectrum analyzer are: SPAN, RBW, VBW. Briefly explain the meaning of these parameters!
10. Sketch an AM modulated signal both in the time-, and frequency domains!
11. Draw the block diagram of a superheterodyne FSK receiver with one IF (intermediate frequency)! What frequency should be set for the LO (local oscillator) if the signal frequency to be received is 915 MHz, and the IF is 10.7 MHz?