Designing With the TRF6900 Single-Chip RF Transceiver

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ABSTRACT

This document explains how to operate the TRF6900 single-chip RF transceiver. It describes the design and selection of the support circuitry present on the evaluation board and provides generic design equations for each section to assist you with your specific system designs.

To review operation and design equations for the TRF4900 single-chip RF transmitter, see applicable transmitter sections of this document (Section 2).

Contents

List of Figures

List of Tables

1 Introduction

The TRF6900 device integrates radio frequency (RF) with digital and analog technologies to form a frequency-agile transceiver for bidirectional RF data links.

1.1 Description

The TRF6900 device operates as an integrated-transceiver circuit for both the European (868−870 MHz), and the North American (902−928 MHz) ISM bands. This device is expressly designed for low-power applications over an operating voltage range of 2.2 V to 3.6 V, and is well suited for battery-powered operation. A key feature of the TRF6900 transceiver is the use of a direct digital synthesizer (DDS) to allow agile frequency setting with fine-frequency resolution. The receiver uses single conversion, for use with either 10.7-MHz or 21.4-MHz IF filters.

The TRF6900 supports frequency-shift keying (FSK)-modulated transmission or reception with bit rates up to 115.2 Kbps.

1.2 Block Diagram/Pinout

Figure 1 shows the TRF6900 transceiver functional block and identifies the input/output terminals.

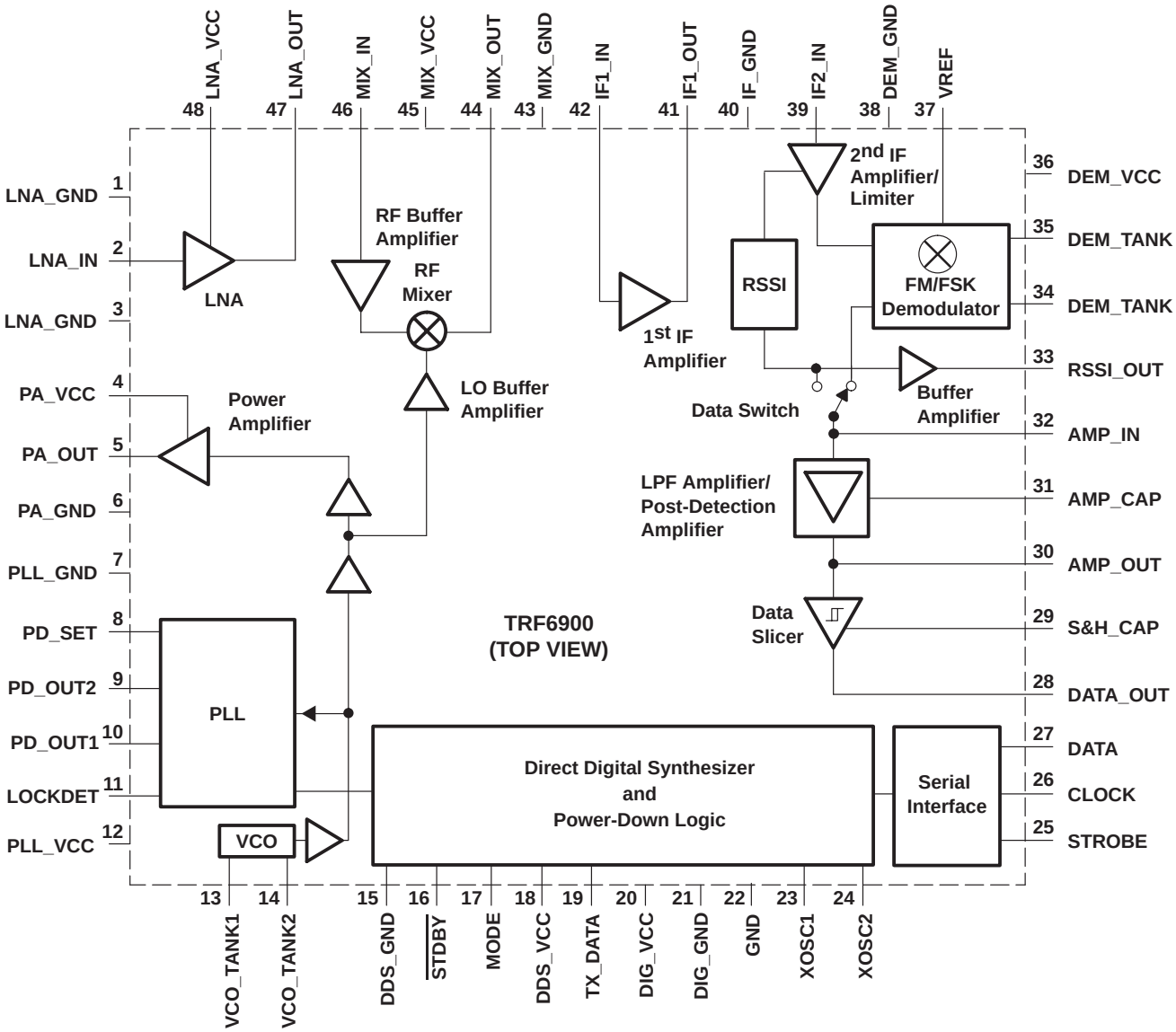


Figure 1. TRF6900 Functional Block Diagram

2 Transmitter

Figure 2 is a block diagram of the TRF6900 that highlights the transmitter portion of the device.

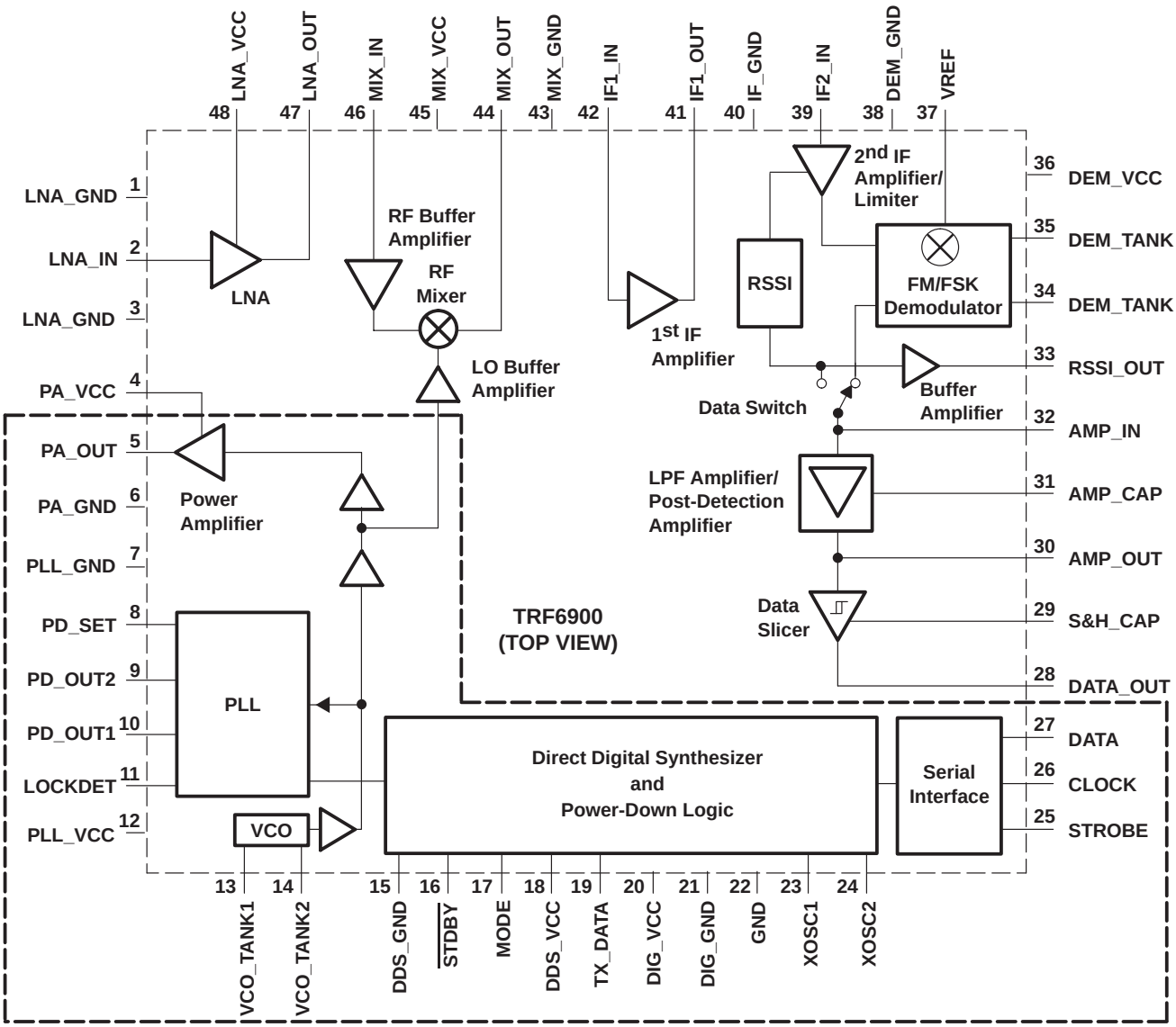


Figure 2. Transmitter Block Diagram

2.1 Direct Digital Synthesizer (DDS) [21] [22]

In general, all frequency synthesizers generate one or many frequencies from a frequency reference, where the synthesized output frequency is related to the reference frequency by a selected ratio. The frequency reference, f_{ref} (which determines the frequency accuracy), is divided to set the step size. This step size is in turn multiplied up to a final output frequency. Characteristics such as operating-frequency range, step size, frequency accuracy, phase noise, switching time, and spurious-signal level are parameters that are balanced to yield a final design. The DDS-based synthesizer simplifies these design issues while maintaining the various performance requirements.

The advantages of using a direct digital synthesizer to drive a phase-locked loop include very fast switching speed and frequency agility with fine frequency resolution, while keeping the design simple and economical. The disadvantages of the DDS-based synthesizer are spurious-signal responses and degradation of phase noise outside the loop bandwidth.

Frequency accuracy is determined by the reference source. For the TRF6900, the reference source is determined by the clock/crystal oscillator circuit. Phase noise in any synthesizer is degraded by 20 Log N. The DDS allows you to reduce N by operating the phase-detector frequency at a much higher reference frequency, while maintaining a finer frequency-resolution in the final output frequency.

Figure 3 on page 8 shows a block diagram of the TRF6900 DDS and synthesizer components. The basic principle of operation of the DDS is to generate a signal in the digital domain and to reconstruct the waveform in the analog domain by D/A conversion. Generation of the signal in the digital domain is accomplished by adders and D-type flip-flops. The D-type flip-flops act as storage devices that change their state when clocked. All arithmetic operations are done using a modulo 2^N, where the N bits determine the output-frequency resolution (f_{pd}) at the phase detector as shown in equation (1).

$$f_{pd} = \frac{f_{ref}}{2^{24}} \quad (1)$$

Where f_{pd} is the minimum phase-detector input frequency. This is the bit weight of the 2^0 bit of the DDS for the clock frequency f_{ref} used. The power in 2^{24} represents the number of registers of the DDS accumulator, which is 24 for the TRF6900.

The value of f_{pd} is multiplied by N, the prescaler value (user-selectable values of 256 or 512), which yields a minimum frequency-step size (Δf) as shown in equation (2) and (3).

$$\Delta f = N \times f_{pd} \quad (2)$$

or

$$\Delta f = N \times \frac{f_{ref}}{2^{24}} \quad (3)$$

As previously mentioned, generation of the signal in the digital domain begins with an accumulator whose output serves as a phase generator. Control inputs to the accumulator are a user-defined frequency word, and a reference clock used to clock the accumulator and other circuits (D/A, etc.). The accumulator output is a series of pulsed digital samples, spaced at the clock rate, in the form of a linear ramp. The slope of this ramped signal represents a phase, based on the user-defined inputs.

The slope of the accumulator output is interpreted as the rate of phase change shown in equations (4) and (5).

$$\text{Phase} = 2 \times \pi \times \left[\frac{(\text{DDS word})}{2^N}\right] \quad \text{Note: This value is in radians.} \tag{4}$$

By taking the derivative of the phase as follows:

$$\omega = \frac{d(\phi)}{d(t)}$$

Where:

$$t = 1/f_{ref} \quad \text{and } \omega = 2\pi f$$

$$f(t) = \frac{\omega}{2\pi}$$

$$\text{Frequency} = (\text{DDS word}) \times \frac{f_{ref}}{2^{24}} \tag{5}$$

This yields a digitally-encoded frequency with a waveform made up of pulsed digital samples spaced at the clock rate and results in a triangular-wave shape.

For example, for a DDS word equal to 2,320,000:

$$\text{Phase} = 2 \times \pi \times \left[\frac{(\text{DDS word})}{2^N}\right] = 2 \times \pi \times \left[\frac{(2,320,000)}{2^{24}}\right]$$

$$= 2 \times \pi \times [0.1382828] = 0.8688563 \text{ radians}$$

$$\omega = \frac{d(\phi)}{d(t)}$$

Where: $t = 1/f_{ref}$

For a 25.6-MHz clock,

$$t = 3.9063 \times 10^{-8} \text{ s}$$

$$\omega = \frac{d(0.8688565 \text{ rad})}{\left(3.9062 \times 10^{-8} \text{ s}\right)}$$

$$\omega = 2.224272 \times 10^7$$

Therefore:

$$f(t) = \frac{\omega}{(2 \times \pi)}$$

$$= \frac{\left(2.2777 \times 10^7\right)}{6.2831853 \text{ rad}}$$

$$= 3.54 \times 10^6 \text{ Hz}$$

An 11-bit digital-to-analog converter (DAC) then converts the generated digital sample (made up of a staircase triangular wave) to an analog form. Due to the quantization processes occurring in the DAC, the resulting output signal is only an approximation of the ideal signal. The output of the DAC contains all the frequency components of the fundamental (that is, harmonics, data glitches, clock leakage) plus their aliases resulting from the sampling process.

Following the DAC, a sine-shaper circuit is used to minimize DAC-signal glitches, etc. The sine-shaper circuit is followed by a 4-MHz antialiasing filter, which minimizes sampling spurs due to the D/A conversion process. The ultimate performance of the DDS is primarily dependent on the quantization errors due to the D/A process, together with the effects of the antialiasing filter that follows the DAC.

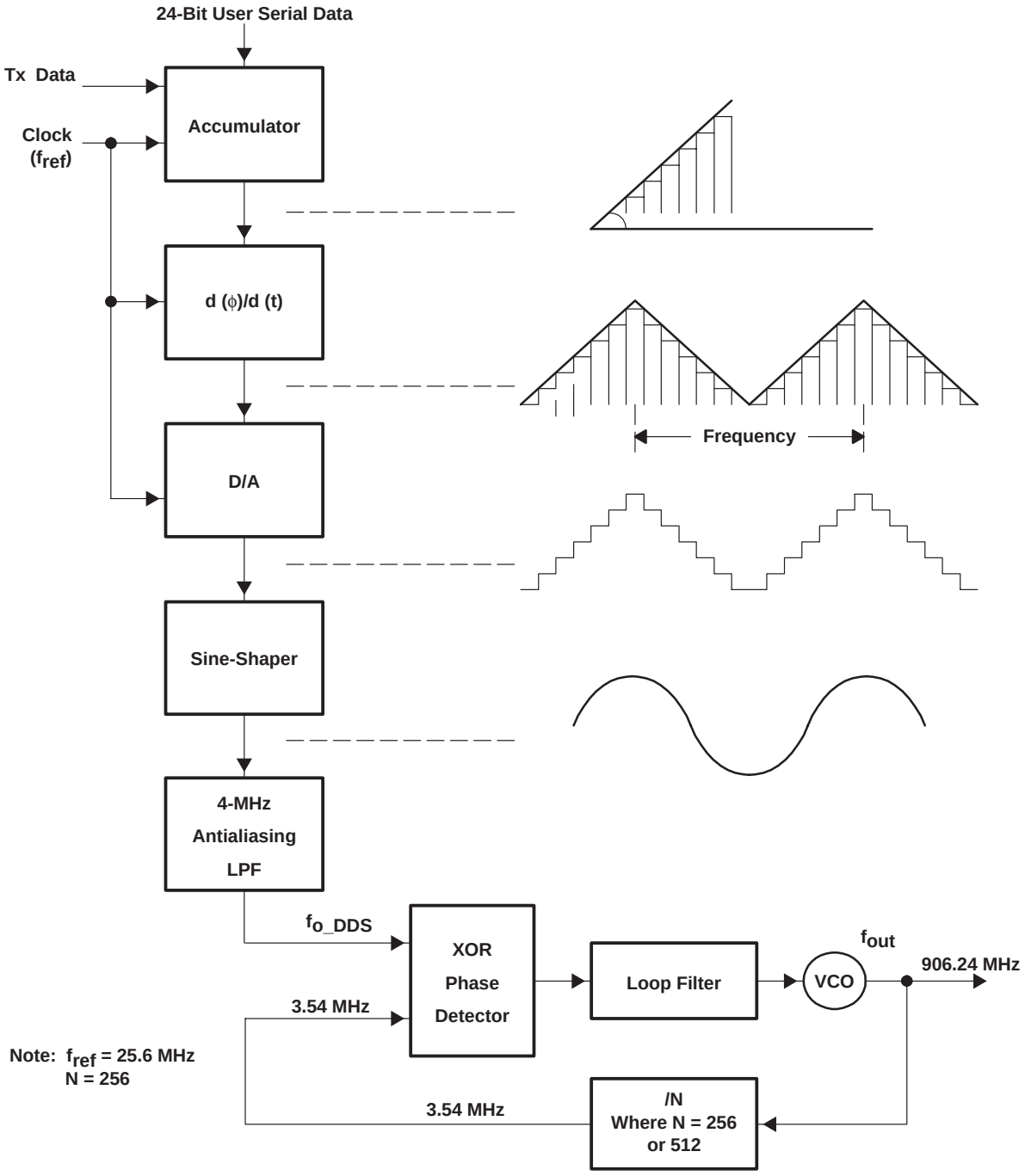


Figure 3. TRF6900 DDS/Synthesizer Block Diagram

The following paragraphs summarize the general performance of the DDS:

- The length of the accumulator and the clock frequency determine the frequency resolution. The accumulator and the clock rate applied to accumulator circuits determine the number of spurious components in the output spectrum.

  Since the accumulator divides by 2^N, it generates a logic-level transition at integer multiples of the clock frequency. The accumulator increments are defined by the DDS frequency word and the clock rate. When the accumulator is forced to make a logic-level transition at some fractional rate, the information contained in the accumulator output versus its carry output produces a phase error or an instantaneous frequency error. Each overflow represents a spurious component in the final output spectrum of the transmitter (TX) or local oscillator (LO). The number of spurious signals can be greatly reduced by proper selection of the clock frequency.

  Another characteristic parameter of the accumulator is data jitter. Generally this is not an issue in low data-rate applications; however, this may become a concern at higher data rates. Jitter results from the accumulator's average frequency error due to the digital ramp. You can influence the jitter performance by reducing the ratio of the DDS frequency word relative to the accumulator length (2^{24}). One possible way to reduce data jitter is the selection of higher input-clock frequencies. As the weight of each accumulator bit is increased, and thus fewer bits are used in the DDS frequency word, the ratio of the DDS frequency word to the accumulator length is reduced.

  Additional factors that affect data jitter are clock stability and insufficient bandwidth in the receiver post-detection amplifier.

The clock frequency (due to sampling theory) influences quantization noise power and spurious-signal levels, as well as the number of aliasing spurs contained in the output spectrum. The higher the f_{ref}/f_{o_DDS} ratio, the lower these effects are in the final output spectrum where f_{ref} is the frequency of the reference clock and f_{o_DDS} is the output frequency of the DDS (in phase lock) defined in equation (6).

$$f_{o\_DDS} = \frac{f_{out}}{N} \tag{6}$$

f_{out} is the output frequency of the VCO where *N* is the divide-by-N factor with a value of 256 or 512. f_{o_DDS} is the input comparison frequency to the phase detector of the TRF6900.

As the clock frequency (or sampling frequency) is increased, both the number and level of the spurious products in the output spectrum are reduced, while final frequency resolution is degraded.

2.2 Clock Frequency Selection [21] [22]

Selection of the clock frequency is key in determining the overall DDS spurious performance. The main issue is to minimize the DDS-generated spurs while allowing the VCO to be programmed to decimal numbers with minimum frequency error. The chosen clock frequency must be sufficiently high that the reference spur frequencies are at large enough offsets from the carrier frequency and the loop contributes to spur suppression. The following demonstrates the selection of the clock frequency and the determination of the synthesizer final output frequency.

Assume an output frequency from a DDS-based synthesizer of 928 MHz. This frequency is the final VCO output, not to be confused with the DDS output frequency at the phase detector. The phase-lock loop (PLL) phase detector has two inputs: a reference frequency from the DDS and a sample output from the VCO, which is divided by a prescaler value of 256 or 512 (user-selectable). The reference input from the DDS is used to steer and hold the VCO at the output frequency that you select (see Figure 3).

For a VCO output of 906.24 MHz, the DDS output frequency is 906.24 MHz/256 = 3.54 MHz. For the PLL to lock the VCO at this frequency, the phase detector reference input from the DDS also must be 3.54 MHz. The DDS output frequency is effectively multiplied by the prescaler value being used in the loop. The frequency of operation for the PLL is calculated as shown in equation (7).

$$f_{out} = \text{(Prescaler)} \times \text{(DDS value)} \times \frac{f_{ref}}{2^{24}} = \text{(N)} \times \text{(DDS\_x)} \times \frac{f_{ref}}{2^{24}} \quad (7)$$

The DDS is programmed by a 24-bit control register, where the LSB bit weight is 2^0 and the MSB bit weight is 2^{23}. The two most significant bits (bits 22 and 23) are not user-accessible and are set to zero internally. Bits 0 through 21 are used to program the transmitter and receiver to the frequencies that you choose.

Table 1 shows an example of the DDS register bit weights versus frequency quantization at the phase detector and VCO outputs. At the phase detector, the quantization value of the MSB is $f_{ref}/2$ (also called the Nyquist frequency). Each additional bit is further divided by 2 to produce the LSB, with $f_{out} = f_{ref}/2^{24}$ (where 24 is the DDS bit-sequence length). As shown in Table 1, $f_{ref}/2^{24}$ = 25,600,000/16,777,216 = 1.525879 Hz, which represents the LSB frequency resolution at the phase detector. Note that the LSB is located in the *Frequency at Phase Detector* column of Table 1. The frequency resolution at the VCO output is this value (1.525879 Hz) times 256, which is equal to 390.625 Hz. Each bit of the DDS register is multiplied by the 1.525879-Hz factor. Each effective bit of the *Frequency at Phase Detector* is further multiplied by the selected prescaler value (256) to yield an effective *Frequency at VCO* quantization value as follows:

Frequency at Phase Detector	**Frequency at VCO**
$2^{21} \times 1.525879$ = 3,200,000 Hz	3,200,000 × 256 = 819,200,000 Hz
$2^{20} \times 1.525879$ = 1,600,000 Hz	1,600,000 × 256 = 409,600,000 Hz
.	.
.	.
$2^{00} \times 1.525879$ = 1.525879 Hz	1.525879 × 256 = 390.625 Hz

The VCO frequency resolution is 390.625 Hz for this clock frequency. Any clock frequency error is reflected directly to the final frequency error. Hence, if the clock frequency error is 10 ppm, then the final output frequency will also have a frequency error of 10 ppm.

The PLL filter bandwidth has very little effect on reduction of DDS spurs, since the DDS spurs appear very close to the carrier. The objective is to choose a clock frequency that yields a minimum number of DDS spurs while allowing the VCO output to yield a minimum frequency error. The recommended clock frequencies of 22, 25.60, and 26 MHz yield minimum spurious components. To ensure a successful application, you must evaluate the selected clock frequency for DDS spurious frequency performance versus the final output frequencies used.

Table 1. Clock Frequency of 25.6 MHz

BIT	BIT WEIGHT OF DDS WORD	FREQUENCY AT PHASE DETECTOR	FREQUENCY AT VCO	FREQUENCY OF 902 MHz	FREQUENCY OF 915 MHz	FREQUENCY OF 928 MHz
$23 = 2^{23}$	8,388,608	12,800,000 Nyquist Frequency	3,276,800,000			
$22 = 2^{22}$	4,194,304	6,400,000	1,638,400,000			
$21 = 2^{21}$	2,097,152	3,200,000	819,200,000	1	1	1
20	1,048,576	1,600,000	409,600,000			
19	524,288	800,000	204,800,000			
18	262,144	400,000	102,400,000			1
17	131,072	200,000	51,200,000	1	1	
16	65,536	100,000	25,600,000	1	1	
15	32,768	50,000	12,800,000		1	
14	16,384	25,000	6,400,000			1
13	8,192	12,500	3,200,000	1	1	
12	4,096	6,250	1,600,000	1	1	
11	2,048	3,125	800,000	1	1	
10	1,024	1,562.500	400,000	1	1	
9	512	781.250	200,000		1	
8	256	390.625	100,000			
7	128	195.312,500	50,000			
6	64	97.656,250	25,000			
5	32	48.828,125	12,500			
$4 = 2^{4}$	16	24.414,063	6,250			
$3 = 2^{3}$	8	12.207,031	3,125			
$2 = 2^{2}$	4	6.103,515,600	1,562.500			
$1 = 2^{1}$	2	3.051,757,800	781.250			
$0 = 2^{0}$	1	1.525,878,900	390.625			
			DDS value =	2,309,120	2,342,400	2,375,680
			PD Frequency =	2,523,438	3,574,218,800	3,625,000

NOTE: Calculated values are based on N = 256.

A DDS programming example (using a 25.6-MHz clock) for a VCO output of 915 MHz is detailed as follows:

DDS Word

2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{09}	2^{08}	2^{07}	2^{06}	2^{05}	2^{04}	2^{03}	2^{02}	2^{01}	2^{00}
0	0	1	0	0	0	1	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0

The value of each bit is summed ($2^{21}+2^{17}+2^{16}+2^{15}+2^{13}+2^{12}+2^{11}+2^{10}+2^{9}$) to yield a DDS value of 2,342,400.

The final output frequency is given in equation (8).

$$f_{out} = (\text{Prescaler}) \times (\text{DDS value}) \times \frac{f_{ref}}{2^{24}} = (N) \times (DDS\_x) \times \frac{f_{ref}}{2^{24}} \quad (8)$$

$$f_{out} = (N) \times (\text{DDS value}) \times \left[\frac{(f_{ref})}{16,777,216}\right] = (256) \times (2,342,400) \times \left[\frac{(25,600,000)}{16,777,216}\right] = (256) \times (3,574,218.800) = 915,000,000 \text{ Hz}$$

2.2.1 Calculation of DDS Word

The binary value of the DDS word (DDS_x) is calculated by solving equation (7) for the decimal value of the DDS word. This value is then converted to hexadecimal format. The hexadecimal value can then be written in binary format to complete the conversion.

Equation (8), as stated in the TRF6900 data sheet, is:

$$f_{out} = (N) \times \frac{f_{ref} \times DDS\_x}{2^{24}} \quad (9)$$

Where:

f_{out}:	VCO output frequency
N:	Divide-by ratio of the prescaler
f_{ref}:	f_{clock} system clock frequency
DDS_x:	DDS word value in decimal format

Solving equation (9) for the DDS word yields:

$$DDS\_x = \frac{\frac{f_{out}}{N} \times 2^{24}}{f_{ref}} \quad (10)$$

The following example uses equation (10) to demonstrate the calculation of the A and B words for FSK modulation.

Example 1. Calculation of the DDS Word

Actual FSK modulation is accomplished by using the dedicated FSK frequency deviation register in the TRF6900. The A and B words then can be used for setting the RX and TX frequencies and for channel hopping. For illustration purposes only, this example shows how to calculate the DDS_x values of the A and B words for an FSK deviation of 20 kHz if the user were to use the A and B words to provide FSK modulation. In actual use, the A and B words would be used for FSK deviation only for high deviations that are not supported by use of the deviation register.

Given: FSK system with carrier frequency of 915.0 MHz and 20-kHz FSK deviation. The system clock is 25.6 MHz, N is 256 for the DDS.

Determine: The DDS_x value of the A and B words

Solution $f_{clock} = f_{ref} = 25.6$ MHz
N = 256
$f_{out1} = 915.00$ MHz A word
$f_{out2} = 915.02$ MHz B word

Calculation of DDS_x value for A word:

The A word has a DDS_x designation of DDS_0.

$$DDS\_0 = \frac{\frac{f_{out1}}{N} \times 2^{24}}{f_{ref}} \tag{11}$$

$$DDS\_0 = \frac{\frac{915.00\ MHz}{256} \times 2^{24}}{25.6\ MHz}$$

$$DDS\_0 = 2.3424 \times 10^6 \text{ decimal}$$

$$DDS\_0 = 23BE00_{hex}$$

$$DDS\_0 = 0010\ 0011\ 1011\ 1110\ 0000\ 0000_{binary}$$

The binary format of DDS_0 is loaded into the A word.

Calculation of DDS_x value for B word.

The B word has a DDS_x designation of DDS_1.

$$DDS\_1 = \frac{\frac{f_{out2}}{N} \times 2^{24}}{f_{ref}} \tag{12}$$

$$DDS\_1 = \frac{\frac{915.02\ MHz}{256} \times 2^{24}}{25.6\ MHz}$$

$$DDS\_1 = 2.342451 \times 10^6 \text{ decimal}$$

Example 1. Calculation of the DDS Word (Continued)

$$DDS\_1 = 23BE33_{hex}$$

$$DDS\_1 = 0010\ 0011\ 1011\ 1110\ 0011\ 0011_{binary}$$

The binary format of DDS_1 is loaded into the B word.

2.3 Crystal Specifications

The following table shows typical crystal specifications. A fundamental-mode crystal is recommended instead of an overtone crystal. The fundamental-mode crystal is used to keep the spurious frequency components of the crystal out of the VCO output spectrum.

Typical Crystal Specifications

Operating frequency (fundamental mode)	25.6000 MHz or 26 MHz
Frequency accuracy	±20 ppm
Load capacitance	20 pF
Shunt capacitance (C_0)	4 pF ±20%
Series resistance	30 Ω maximum
Stability	±20 ppm (−40°C to 85°C)
Aging	5 ppm/year
Typical package	HC-45/U GW

One concern is the required frequency accuracy of the crystal, which must be determined by the application requirements.

The frequency error is of less concern when it is small in relation to the receiver IF filter bandwidth. Conversely, in applications where the frequency error is large with respect to the IF filter bandwidth, such as when narrow IF bandwidth filters are used (that is, 30 kHz), the frequency error becomes a concern.

The frequency error of the reference source is reflected at the output of the VCO as shown in Table 2:

Table 2. Frequency Error vs ppm

VCO OUTPUT FREQUENCY	TOLERANCE OF CRYSTAL (ppm)	FREQUENCY ERROR
915 MHz	±1.0 ppm	±915.0 Hz
915 MHz	±10.0 ppm	±9.150 kHz
915 MHz	±50.0 ppm	±45.750 kHz
915 MHz	±100.0 ppm	±91.50 kHz

Therefore, if the frequency of the reference clock is off by 10 ppm, the VCO output frequency will be off by 10 ppm. In a typical communications link, this frequency error results in a degradation of the receiver sensitivity.

The frequency error can be held to a minimum by a simple automatic frequency control (AFC). Typical consumer designs use a manual frequency adjustment to align the crystal reference frequency. Another approach is to measure the reference frequency error, and then use software control to add a frequency offset to correct it. If a software frequency offset is used, the crystal tolerance can be degraded to 20, 50, or 100 ppm. The software frequency offset can make the crystal accuracy independent of final output-frequency error. Another benefit of adding a software frequency offset is the reduction in DDS spurs. If the DDS D/A is set to an exact submultiple of the clock frequency, then the quantization noise is concentrated at multiples of the output frequency. If the clock frequency is offset in the software by the clock crystal's frequency error, the quantization noise is random, resulting in an improvement of DDS spur levels.

An error of 10 to 20 ppm is acceptable for IF bandwidths of 100 kHz or more. If the application requires IF bandwidths of 30 kHz to 50 kHz, a crystal with better than 10-ppm frequency accuracy may be required.

2.4 TRF6900 Clock Circuit

The TRF6900 clock-oscillator circuit is shown in Figure 4. This circuit uses the crystal in a parallel-resonant mode.

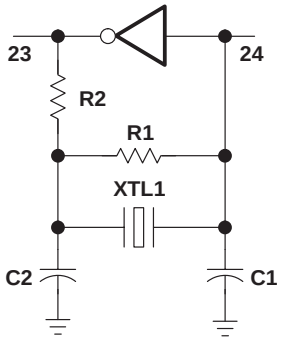


Figure 4. Clock Circuit

The total phase shift around the loop is 360 degrees, with the inverter providing 180 degrees of phase shift. Resistor R_2 and capacitor C_2 provide a 90-degree phase lag, and the crystal and capacitor C_1 provide an additional 90-degree phase lag. In reality, the inverter provides less than 180 degrees of phase shift due to its internal capacitance. The R_2-C_2 combination also provides something less than 90 degrees of phase shift. The crystal is operating in parallel-resonant mode and acting as an inductor. The crystal-load capacitance makes up the additional phase shift required for oscillation (360 degrees).

Bias resistor R_1 sets the bias point for the inverter, which is typically one-half of V_{CC}. Low values of R_1 reduce the loop gain and disturb the phase of the feedback network. Typical values for R_1 are 1 MΩ to 5 MΩ.

Crystal-drive resistor R_2 is used to limit the crystal drive level by forming a voltage divider between R_2 and C_2. To verify that the maximum operating supply voltage does not overdrive the crystal, observe the output frequency as a function of voltage at terminal 23. Under proper operating conditions, the frequency should increase slightly (a few ppm) as the supply voltage increases. If the crystal is being overdriven, an increase in supply voltage causes a decrease in frequency; if this happens, increase the value of R_2. In addition, the value of R_2 must be sufficiently low to ensure that the oscillator starts at a few tenths of a volt below the minimum operating voltage.

Ideally, capacitor C_2 together with drive resistor R_2 provide 90 degrees of phase shift and set the crystal-drive level. Large values of C_2 tend to stabilize the oscillator against variations in V_{CC}, while also reducing any overtone activity of the crystal. Capacitor C_1 and the internal impedance of the crystal provide an additional 90 degrees of phase shift. Large values of C_1 reduce loop gain while increasing frequency stability. The series sum of capacitor C_1, the crystal's shunt capacitance (C_0), and the input capacitance of the inverter gate make up the crystal's load capacitance. For increased stability, the load capacitance of the crystal should have a typical value of approximately 20 to 30 pF.

2.5 Local Oscillator

The local oscillator (LO) of the TRF6900 ISM transceiver is a phase-locked loop (PLL) consisting of an on-chip DDS-based frequency synthesizer, an external passive-loop filter, and a voltage-controlled oscillator (VCO). The general functional block diagram of the local oscillator is shown in Figure 5.

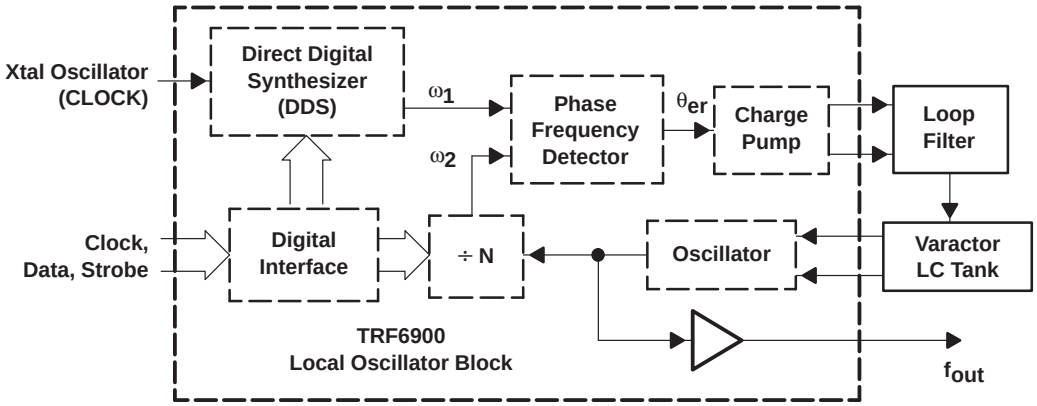


Figure 5. TRF6900 Local Oscillator Functional Block Diagram

The following sections detail the design considerations for the TRF6900 phase-locked loop (PLL).

2.5.1 Voltage-Controlled Oscillator

2.5.1.1 Varactor LC Tank Design

Figure 6 describes the VCO of the TRF6900 ISM transceiver, the on-chip oscillator, and an external differential varactor LC tank. As shown in Figure 6, the resonant frequency of the tank is given in equation (13).

$$f_{TANK} = \frac{1}{2\pi\sqrt{LC_{TOTAL}}} \tag{13}$$

The total capacitance C_{TOTAL} of equation (13) is defined in equation (14).

$$C_{TOTAL} = C_5 + \frac{1}{\frac{1}{C_{34}} + \frac{1}{C_{34}} + \frac{1}{C_{VR1}} + \frac{1}{C_{VR2}}} \tag{14}$$

where $C_{34} = C_3 = C_4$

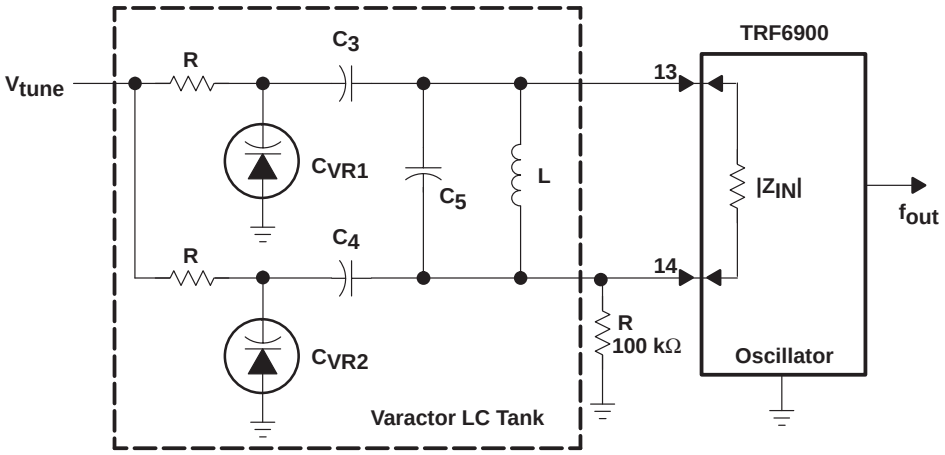


Figure 6. Voltage-Controlled Oscillator for the TRF6900 ISM Transceiver

At the resonant frequency, the required inductor value for the differential tank shown in Figure 6 is calculated in equation (15).

$$L = \frac{1}{2} \times \frac{\frac{|Z_{IN}| \times Q_P}{Q_{LOADED}} - |Z_{IN}|}{2\pi f \times Q_P} \quad (15)$$

Where:

$\|Z_{IN}\|$:	Input impedance of the oscillator
Q_{LOADED}:	Quality factor of the tank
Q_P:	Quality factor of the inductor
f:	Desired resonant frequency

To maximize the frequency tuning range of the tank via the varactor, equation (17) dictates that a small value for the capacitor C_5 must be chosen, and capacitors C_3 and C_4 must be as large as possible. With C_5 small, the C_5 term in equation (17) may be negligible. If C_3 and C_4 are as large as possible, the terms $\frac{1}{C_3}$ and $\frac{1}{C_4}$ are also negligible. Therefore, the variation of C_{TOTAL} would be dominated by C_{VR1} and C_{VR2}.

Note that the stray capacitance due to the printed-circuit board (PCB) layout is virtually in parallel with the total capacitance of the tank, and does not affect its resonant frequency. Capacitor C_5 must be carefully chosen to include the stray capacitance. If the stray capacitance strongly affects the resonant frequency of the tank, the value of C_5 may be reduced through experimentation with the actual circuit on the PCB.

Assuming that $C_{34} = C_3 = C_4$, and $C_{VR} = C_{VR1} = C_{VR2}$, the relationship of capacitors C_{34} and C_{VR} is described in equation (16).

$$C_{VR} = \frac{C_{34} \times 2\left(C_{TOTAL} - C_5\right)}{C_{34} - 2\left(C_{TOTAL} - C_5\right)} \quad (16)$$

Due to the availability of the tuning capacitance range of the varactor versus the available tuning voltage, capacitor C_{34} is arbitrarily chosen at the center frequency of the desired frequency range. The typical value of capacitor C_{34} needs to satisfy the following condition, as shown in equation (17).

$$C_{34} \geq 2 \times \left(C_{TOTAL} - C_5\right) \tag{17}$$

Remember that the value of capacitor C_{34} should be as large as possible; thus the $\frac{1}{C_{34}}$ term in equation (14) is negligible. Subsequently, the variation of C_{TOTAL} is then dominated by C_{VR}.

In any application where the TRF6900 is powered up continuously in either TX or RX mode without periodically going into STBY mode, it is recommended that a 100-kΩ resistor be added to the VCO tank from either terminal 13 or terminal 14 to ground to ensure the long-term stability of the V_{tune} voltage.

The addition of the 100-kΩ resistor to the VCO tank tends to shift the operating frequency of the VCO downward and decrease K_{VCO}. Thus, after calculation of the VCO components some fine tuning may be needed to re-center the tuning range.

2.5.1.2 VCO Sensitivity

Assuming that the capacitance of the varactor varies linearly with the tuning voltage, the sensitivity of the VCO is defined in equation (18).

$$K_{VCO} = \frac{\Delta f}{\Delta V_{tune}} \tag{18}$$

where $\Delta f = | f_1 - f_2 |$, and $\Delta V_{tune} = |$ V_{tune} at $f_1 - V_{tune}$ at $f_2 |$

2.5.1.3 Numerical Calculation

The VCO of the TRF6900 initially is designed to operate between 880 MHz and 950 MHz with a tuning voltage range of less than 0.3 V to approximately 3 V. The input impedance $|Z_{IN}|$ of the oscillator between terminals 13 and 14 is approximately 1400 Ω. The loaded Q of the tank, Q_{LOADED}, must be equal to or greater than 10. The selected inductor (LQW1608A series from muRata) has a quality factor Q_P of approximately 80 at 915 MHz.

The required inductor for the tank is calculated from equation (15) as:

$$L = \frac{1}{2} \times \frac{\frac{|Z_{IN}| \times Q_P}{Q_{LOADED}} - |Z_{IN}|}{2\pi f \times Q_P} = \frac{1}{2} \times \frac{\frac{1400 \times 80}{\geq 10} - 1400}{2 \times 3.1416 \times 915e6 \times 80} \leq 10.65 \text{ nH}$$

Choose L = 10 nH, a standard value.

From equation (13), the required total capacitance (C_{TOTAL}) is:

$$\text{At } f_1 = 880 \text{ MHz}: \quad C_{TOTAL\_f1} = \frac{1}{(2\pi \times 880e6)^2 \times 10e-9} \approx 3.271 \text{ pF}$$

$$\text{At } f_c = 915 \text{ MHz}: \quad C_{TOTAL\_fc} = \frac{1}{(2\pi \times 915e6)^2 \times 10e-9} = 3.025 \text{ pF}$$

$$\text{At } f_2 = 950 \text{ MHz}: \quad C_{TOTAL\_f2} = \frac{1}{(2\pi \times 950e6)^2 \times 10e-9} = 2.807 \text{ pF}$$

To maximize the frequency tuning range of the tank via the varactors, the capacitor C_5, which includes any PCB stray capacitance, is chosen to be 2.2 pF for this calculation and, from equation (16), C_{34} is chosen to be 3.3 pF to mate with a varactor having the following characteristics:

$$\text{At } V_{tune} \le 0.5 \text{ V}: \quad C_{VR} \ge \frac{3.3e-12 \times 2(3.271e-12 - 2.2e-12)}{3.3e-12 - 2(3.271e-12 - 2.2e-12)} = 6.103 \text{ pF}$$

$$\text{At } V_{tune} \le 2 \text{ V}: \quad C_{VR} \le \frac{3.3e-12 \times 2(2.807e-12 - 2.2e-12)}{3.3e-12 - 2(2.807e-12 - 2.2e-12)} = 1.919 \text{ pF}$$

An SMV1247 varactor from Alpha Industries is chosen. This varactor has the following characteristics:

$C_{VR} \approx 8.50$ pF at $V_R = 0.10$ V
$C_{VR} \approx 7.50$ pF at $V_R = 0.25$ V
$C_{VR} \approx 3.66$ pF at $V_R = 1.25$ V
$C_{VR} \approx 1.88$ pF at $V_R = 2.00$ V
$C_{VR} \approx 0.90$ pF at $V_R = 3.00$ V

Note that the PCB stray capacitance is unknown, difficult to predict, and varies with operating frequency. Therefore, empirical measurement may be required to define the value of C_5.

Verification:

With selected values, the total capacitance of the tank is calculated using equation (14) as:

$$\text{At } f_{tune} = 0.10 \text{ V}:$$
$$C_{TOTAL} = 3.39 \text{ pF}$$

$$\text{At } f_{tune} = 0.25 \text{ V}:$$
$$C_{TOTAL} = 2.2e-12 + \frac{1}{\frac{1}{3.3e-12} + \frac{1}{3.3e-12} + \frac{1}{7.5e-12} + \frac{1}{7.5e-12}} = 3.346 \text{ pF}$$

$$\text{At } f_{tune} = 2.00 \text{ V}:$$
$$C_{TOTAL} = 2.2e-12 + \frac{1}{\frac{1}{3.3e-12} + \frac{1}{3.3e-12} + \frac{1}{1.88e-12} + \frac{1}{1.88e-12}} = 2.799 \text{ pF}$$

$$\text{At } f_{tune} = 3.00 \text{ V}:$$
$$C_{TOTAL} = 2.55 \text{ pF}$$

Using equation (13), the resonant frequency of the tank is:

$$f_{1\_TANK\ a} = \frac{1}{2\pi\sqrt{LC_{TOTAL}}} = \frac{1}{2\pi\sqrt{10e-9 \times 3.39e-12}} \approx 864\ MHz$$

$$f_{1\_TANK\ b} = \frac{1}{2\pi\sqrt{LC_{TOTAL}}} = \frac{1}{2\pi\sqrt{10e-9 \times 3.346e-12}} \approx 870\ MHz$$

And

$$f_{2\_TANK\ a} = \frac{1}{2\pi\sqrt{LC_{TOTAL}}} = \frac{1}{2\pi\sqrt{10e-9 \times 2.799e-12}} \approx 951\ MHz$$

$$f_{2\_TANK\ b} = \frac{1}{2\pi\sqrt{LC_{TOTAL}}} = \frac{1}{2\pi\sqrt{10e-9 \times 2.55e-12}} \approx 995\ MHz$$

Which satisfies the required frequency tuning range above 880 MHz and below 940 MHz.

Summary:

The initial component values for the tank to resonate from 880 MHz to 940 MHz are:

L = 10 nH
$C_{34} = C_3 = C_4 = 3.3$ pF
$C_5 = 2.2$ pF

Varactor = SMV1247−079 (Alpha Industries)

Laboratory measurements indicate that if a capacitor C_5 of 2.2 pF is installed on the EVM, the frequency of the VCO simply shifts downward. Thus, the stray capacitance of the PCB affects the resonant frequency of the tank. Capacitor C_5 was omitted on the EVM to correct for the downward shift in resonant frequency.

After the addition of the 100-kΩ resistor to the VCO, C_4 was changed to 2.7 pF to re-center the tuning range. The resultant final values for the VCO tank are:

L = 10 nH
$C_3 = 3.3$ pF
$C_4 = 2.7$ pF

The typical performance of the VCO is illustrated in Figure 7.

Using equation (18), the VCO sensitivity is calculated as:

$$K_{VCO} = \frac{\Delta f}{\Delta V_{tune}} = \frac{951\ MHz - 870\ MHz}{2\ V - 0.25\ V} \approx 46\ MHz/V$$

After the addition of the 100-kΩ resistor to the VCO and finalization of the VCO tank component values, K_{VCO} was found to be ~30 MHz/V.

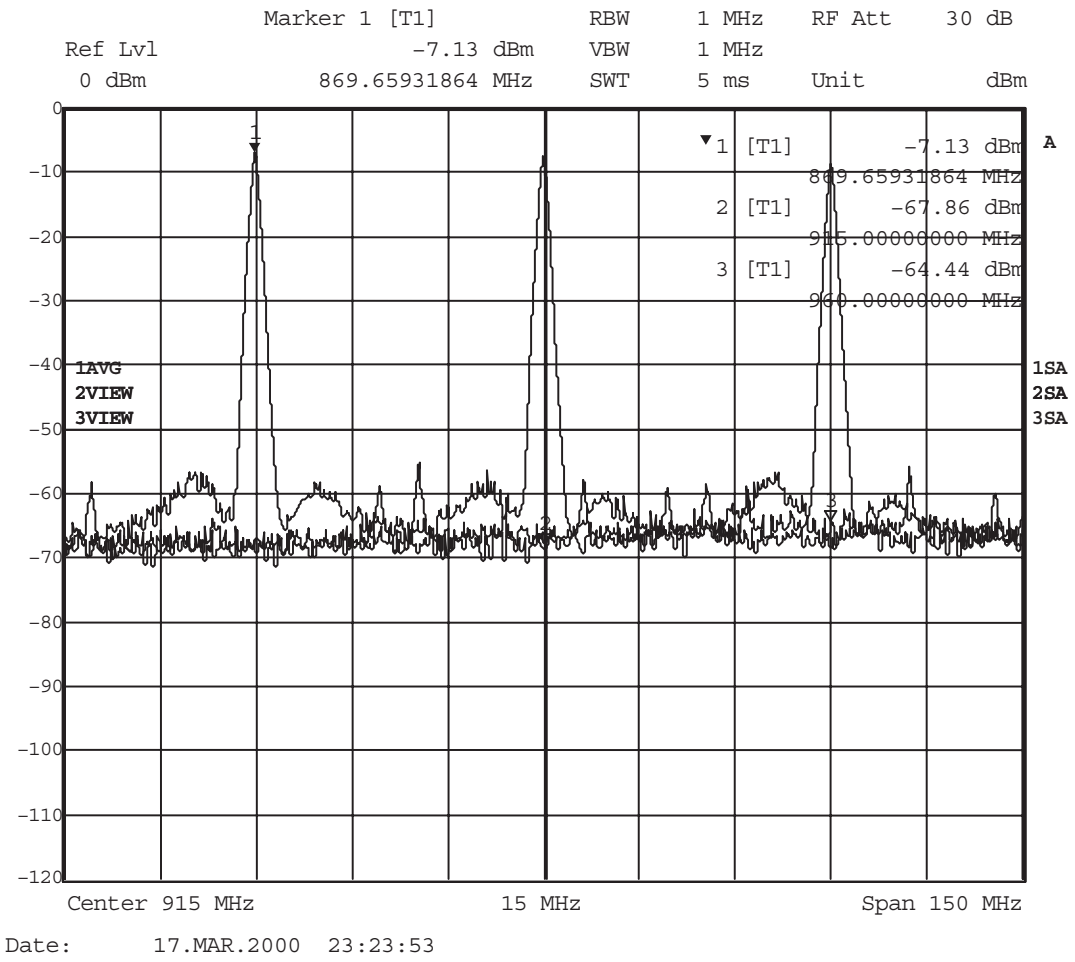


Figure 7. Typical Performance of the VCO

2.5.2 Loop Filter Design

Figure 8 shows a typical second-order passive loop filter configuration commonly used with current-mode charge-pump frequency synthesizer devices.

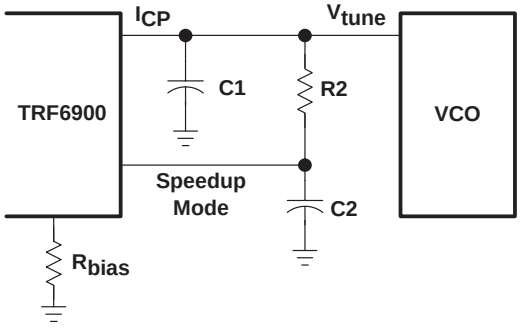


Figure 8. Typical Second-Order Passive-Loop Filter

The component values for this filter are given by the following equations:

$$C_1 = \frac{\tau_1}{\tau_2} \times \frac{K_{PD} \times K_{VCO}}{\omega_c{}^2 \times N} \times \sqrt{\frac{1 + \left(\omega_c \times \tau_2\right)^2}{1 + \left(\omega_c \times \tau_1\right)^2}} \tag{19}$$

$$C_2 = C_1 \times \left[\frac{\tau_2}{\tau_1} - 1\right] \tag{20}$$

$$R_2 = \frac{\tau_2}{C_2} \tag{21}$$

Where:

K_{PD}: Phase-detector gain, $\frac{4 \times I_{CP}}{\pi}$; A/rad

I_{CP}: $I_{CP} = \frac{1.28}{R_{bias}}$

K_{VCO}: VCO gain, $2\pi\frac{\Delta f}{\Delta V_{tune}}$; $\frac{\text{rad/s}}{\text{V}}$

N: Divider constant

R_{bias}: Bias resistor connected to terminal 8

ω_c: Loop bandwidth in radians/s

B_N: $B_N \approx 2 \times$ data rate, Hz

τ_1: $\tau_1 = \frac{\sec\Phi - \tan\Phi}{\omega_c}$

τ_2: $\tau_2 = \frac{1}{\omega_c{}^2 \times \tau_1}$

Φ: Phase margin in radians

2.5.2.1 Numerical Calculation of the Second Order Loop Filter

The divider is selected as N = 256. R_{bias} is selected to be 300 kΩ. The VCO gain was measured as 30 MHz/V.

The loop bandwidth in radians per second is derived in equation (22).

$$\omega_c = 2\pi B_N$$
$$\omega_c = 2\pi \times 20 \times 10^3 \text{ radians/s} \quad (22)$$

where B_N is the recommended loop bandwidth.

The minimum loop bandwidth, in Hertz, must be equal to or greater than the data rate. As a rule of thumb, the loop bandwidth is set to approximately 1.3 to 2 times the data rate. For this example, the loop bandwidth, B_N, was set to 20 kHz, which is twice the data rate (data rate = 10 kHz, bit rate = 20 kbps). A loop bandwidth of 20 kHz should support data rates up to 20 kHz (bit rate = 40 kbps).

The phase margin is set to 50 degrees; thus: $\Phi = \frac{50 \times \pi}{180} = 0.873$ radians.

$$\tau_1 = \frac{\sec\Phi - \tan\Phi}{\omega_c} = 2.896 \times 10^{-6}$$

$$\tau_2 = \frac{1}{\omega_c{}^2 \times \tau_1} = 2.186 \times 10^{-5}$$

From equation (19), capacitor C_1 becomes 92 pF.

From equation (20), capacitor C_2 is found to be 655 pF.

Finally, from equation (21), resistor R_2 is calculated to be 33 kΩ.

Because the calculated component values are not standard, the following standard values are initially selected:

C_1 = 100 pF
C_2 = 650 pF
R_2 = 33 kΩ

Next, the loop values were checked with the following equations:

$$f_n = \text{natural loop frequency} = \frac{1}{2\pi}\sqrt{\frac{K_{PD} \times K_{VCO}}{N \times (C_1 + C_2)}};\ \text{Hz}$$

$$\zeta = \text{loop damping factor} = \frac{R_2 \times C_2}{2} \times 2\pi f_n$$

$$f_c = \text{calculated loop bandwidth} = 2 \times \zeta \times f_n;\ \text{Hz}$$

$$\omega_c = 2\pi f_c$$

The initial values of the loop components were optimized to minimize phase noise and spurious responses, to adjust the loop bandwidth closer to 20 kHz, and to obtain a damping factor close to 1. Normally, the damping factor is set between 0.707, for best switching speed, and 1, for best loop stability. For a damping factor of ζ = 1, the final values selected for the loop filter were:

C_1 = 100 pF
C_2 = 750 pF
R_2 = 39 kΩ

For data rates of 57.6 kbps or higher, an R_{bias} resistor of 200 kΩ is recommended in order to have sufficient charge-pump gain.

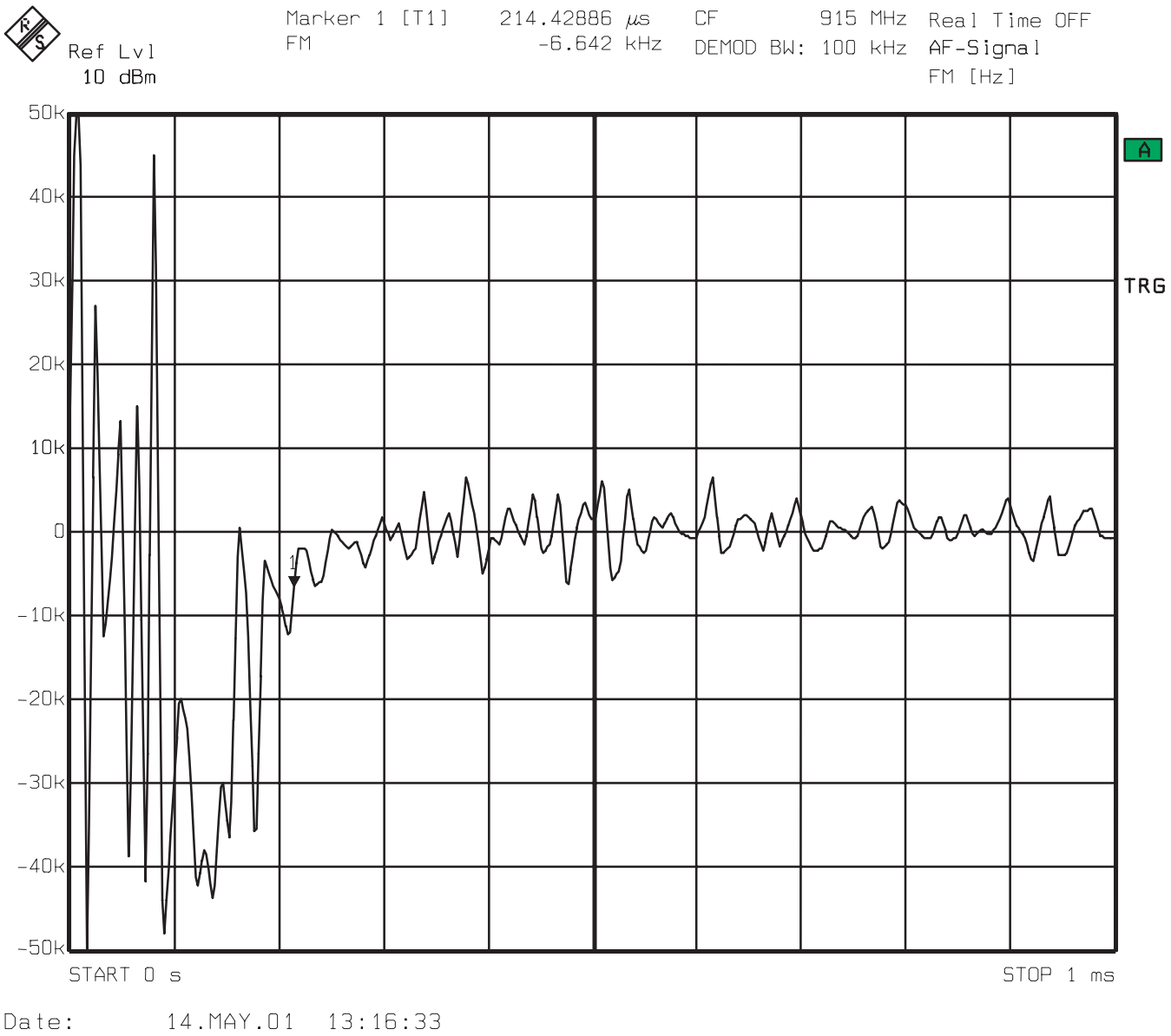


Figure 9. Typical Lock Time Results for a Step of 10.7 MHz

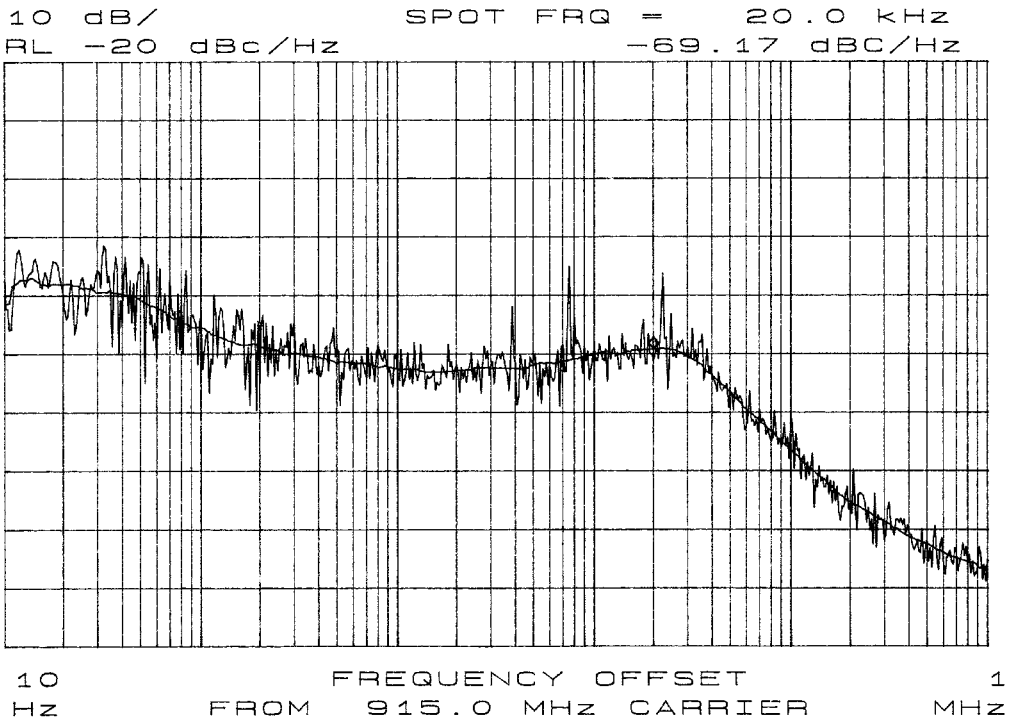


Figure 10. Typical Phase Noise Performance of the PLL

The loop filter receives two inputs from the phase detector: normal mode (terminal 10) and speed-up mode (terminal 9).

Normal mode is used to fine steer and hold the VCO at the commanded frequency.

The speedup mode provides a fast coarse steering of the VCO with the APLL (acceleration factor for PLL) setting. The TRF6900 software allows you to adjust this value as required. The default value is 140 pulses of acceleration; lower values of APLL slow the lock time. When lower values of APLL are used, typical applications are in narrow-band FSK to avoid lock-time overshoot.

Figure 11 details the relationship between the synthesizer loop bandwidth and the TX data rate. For a DDS-based synthesizer, the loop bandwidth must be at least equal to, and preferably greater than, the TX data rate (or modulation rate). As a rule of thumb, for the TRF6900, the loop bandwidth, in Hertz, is set to approximately 1.3 to 2 times the data rate. If this requirement is not met, the FSK output spectrum is distorted. If the loop bandwidth is much less than the TX data rate, no modulation will be present on the output spectrum. Thus, the maximum user data rate determines the minimum loop bandwidth for the application.

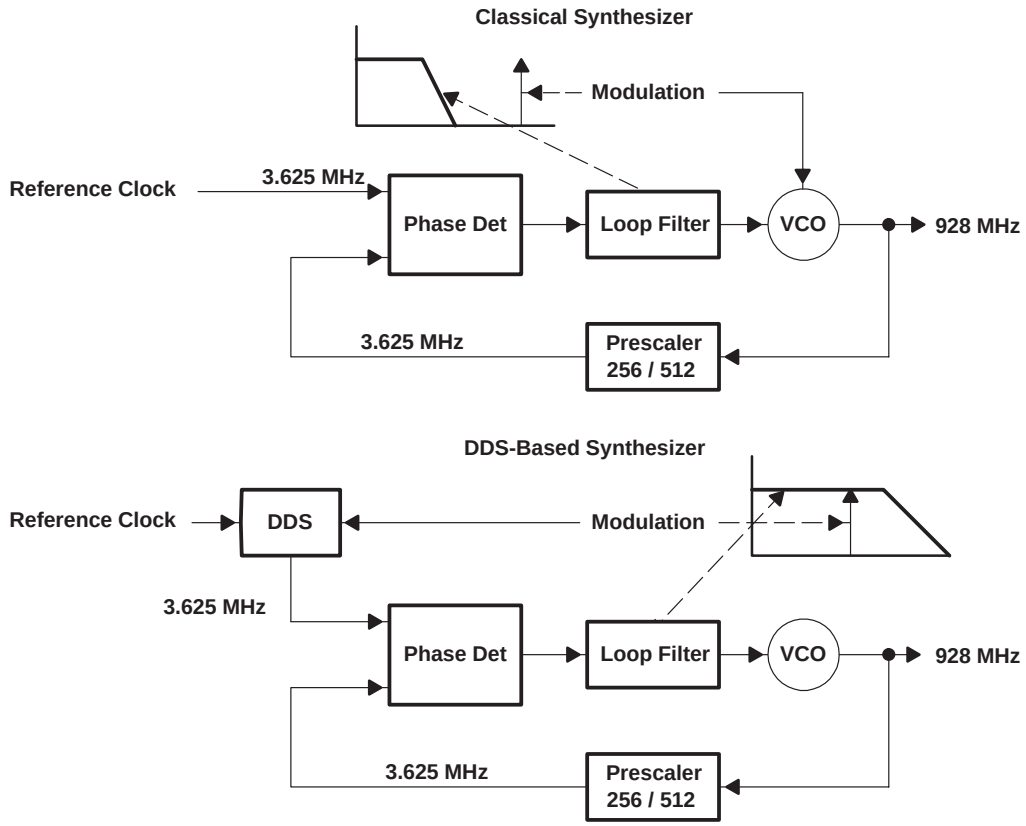


Figure 11. TX Data Rate vs PLL Bandwidth

For the classical synthesizer, which directly modulates the VCO, the modulation rate must be greater than the bandwidth of the PLL loop filter; otherwise, the PLL tends to track out the modulation. With low-frequency modulation, the bandwidth of the PLL loop filter becomes narrow and the resultant lock time of the PLL loop becomes large. Another source of error is when the modulation data contains long strings of ones or zeroes. The problem with a long string of ones or zeroes in the receiver section is that the sample and hold capacitor, which provides the reference level for the data slicer, is not charged to the proper level. Therefore, a Manchester encoding scheme must be used to minimize the modulation tracking problem when the classical synthesizer is used. See Sections 3.8, 3.9, 4, and 4.1 for a more detailed explanation.

A DDS-based synthesizer, as used in the TRF6900, is modulated outside the loop by modulating the reference frequency. As stated previously, the PLL loop bandwidth must be equal to or greater than the modulation rate applied to the synthesizer. The advantage of using a DDS-based synthesizer is that as the PLL loop bandwidth is increased for higher data rates, lock time decreases and close-in phase noise performance improves. The trade-off is that spur suppression and rejection of out-of-band phase noise degrade as the PLL loop-filter bandwidth is increased.

2.6 PLL Phase Noise

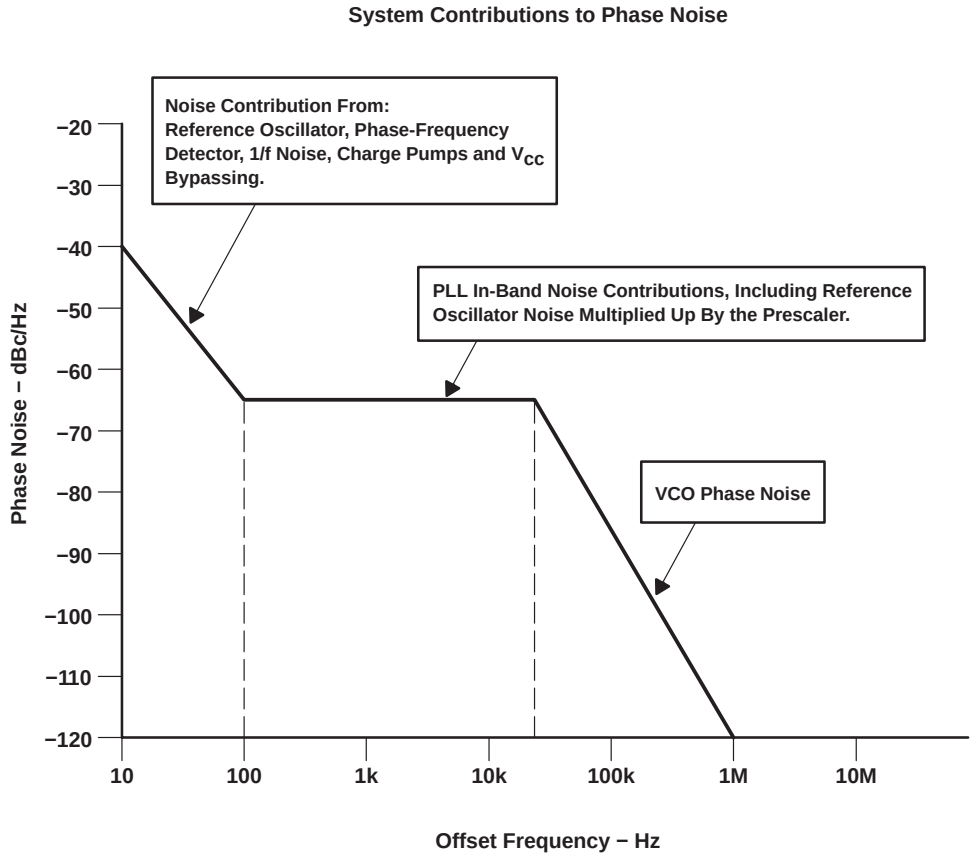


Figure 12. System Phase-Noise Contributions

A typical phase-noise plot, illustrated in Figure 12, comprises three main groups of noise contributors (shown from left to right in order of increasing frequency-offset from the fundamental).

- The IC phase/frequency detector (PFD), charge pump (CP), reference oscillator, 1/f noise, and Vcc bypassing
- The PLL loop filter
- The VCO

The close-in (close to the origin or zero offset) phase noise (1/f noise) is dependent upon the phase/frequency detector and charge pump. The center of the phase-noise plot (in-band) is dependent on the PLL loop bandwidth. The tail of the phase-noise plot (out-of-band) is dependent on the VCO.

Given the above information, the following conclusions can be stated about the effects of changing the loop filter bandwidth for a PLL.

- Wide PLL loop-filter bandwidth has the following results:
  - Decreased close-in phase noise
  - Fast lock time
  - Degraded (less) reference spur suppression
  - Degraded suppression of out-of-band phase noise (high out-of-band phase noise)
- A narrow PLL-filter bandwidth has the following results: (opposite of above)
  - Degraded (increased) close-in phase noise
  - Slow lock time
  - Increased reference spur suppression
  - Increased suppression of out-of-band phase noise

DDS spurs are usually close-in, inside the PLL loop bandwidth, and thus can not be suppressed by the PLL loop filter. However, if we narrow the loop filter bandwidth we can reduce the likelihood that in-band DDS spurs occur. Only proper selection of the reference clock frequency has an influence on DDS spurs. Reference spurs, on the other hand, are generated at integer multiples of the phase-detector input-frequency offset from the carrier frequency and can be filtered by the PLL loop filter.

3 Receiver

The receiver on the TRF6900 is intended to be used as a single-conversion FSK receiver. The receiver is composed of a low-noise amplifier (LNA), mixer, IF amplifier, limiter, an FM/FSK demodulator with an external LC-tank circuit, and a data slicer. Figure 13 is a block diagram of the TRF6900 that highlights the receiver portion of the device.

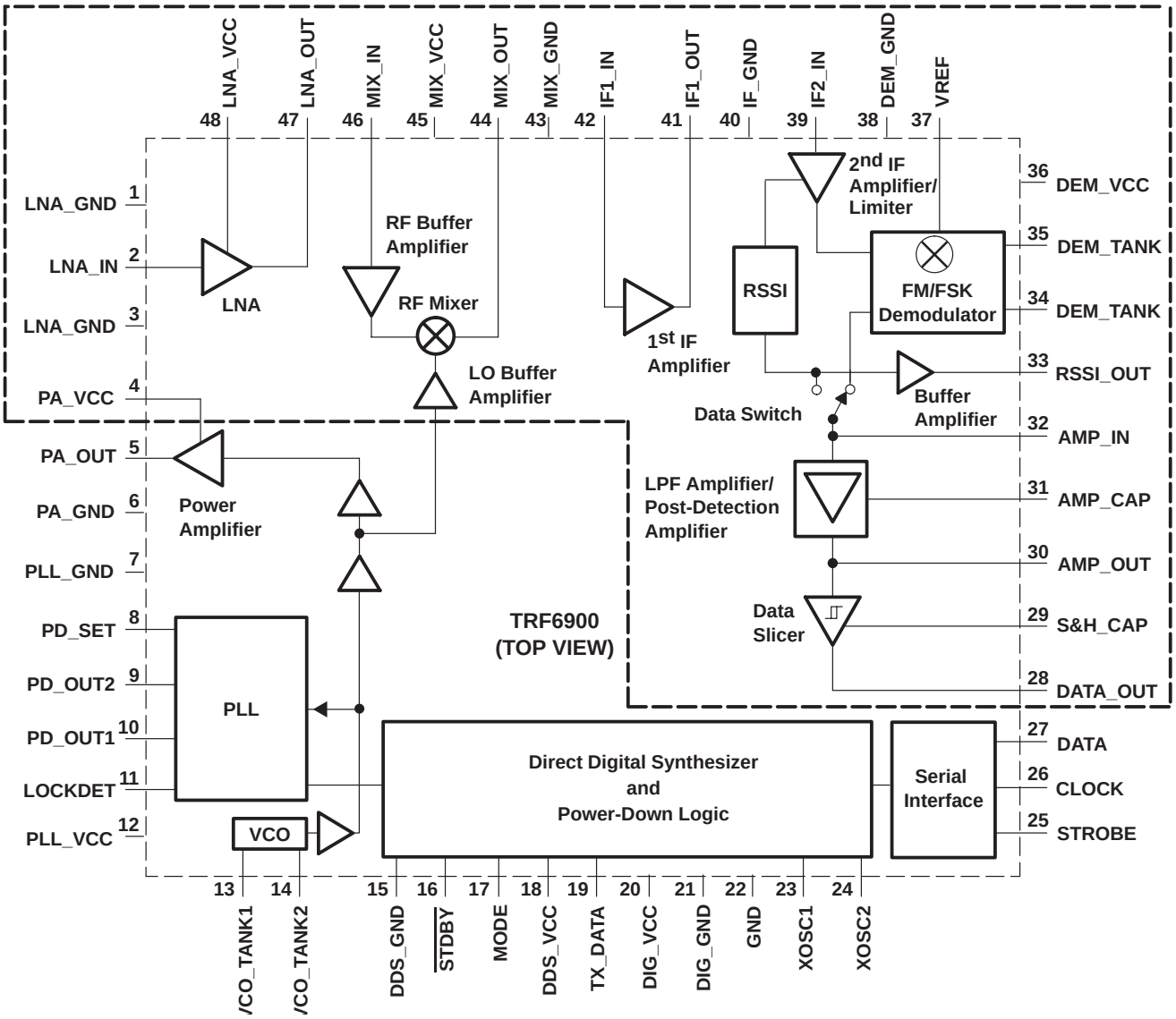


Figure 13. Receiver Block Diagram

3.1 Low-Noise Amplifier (LNA) [22]

The low-noise amplifier (LNA) has a typical gain of 13 dB and a typical noise figure of 3.3 dB. Two operating modes are available for the LNA: normal and low-gain. The normal mode is selected for maximum receiver input sensitivity at low RF input levels. If high RF input levels are to be applied to the LNA, the low-gain mode should be selected.

3.2 Mixer [22]

The mixer is a conventional double-balanced Gilbert-cell mixer. The mixer is designed to operate with the on-chip VCO. When an external LO is desired, an LO drive level of approximately –10 dBm is applied to the VCO input terminal 14 (VCO_TANK2).

The mixer output impedance at terminal 44 (MIX_OUT) is 330 Ω. This impedance allows a ceramic filter with a 330-Ω impedance to be connected directly to terminal 44 (MIX_OUT). Figure 14 shows the LNA and mixer matching circuit components used on the evaluation board. See the *TRF6900 Evaluation Board User's Guide*, literature number SWRU001, for an explanation of its jumper settings.

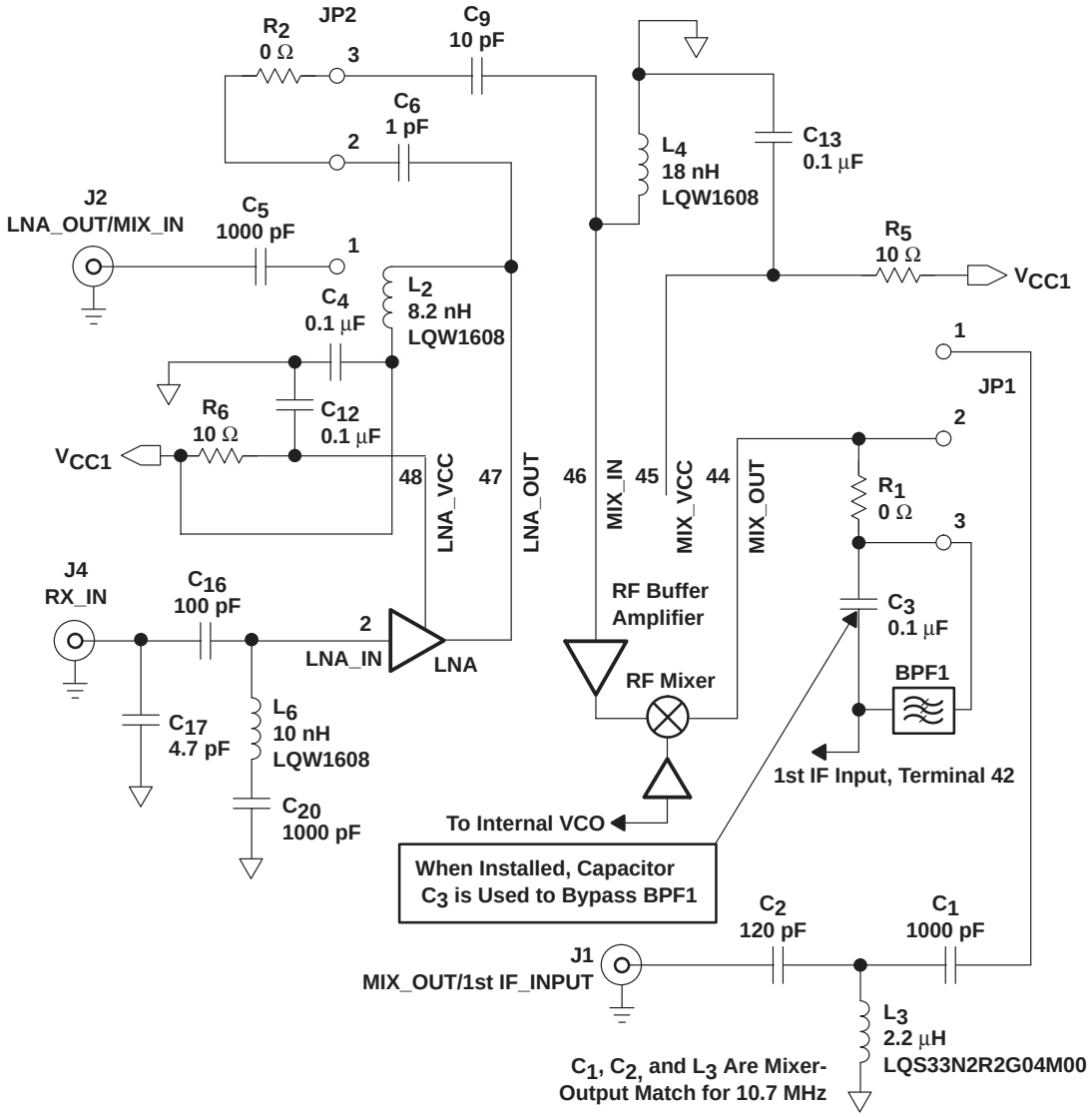


Figure 14. LNA and Mixer Matching Components

3.3 First IF Amplifier [22]

The first IF amplifier has a typical gain of approximately 7 dB, and input and output impedances of 330 Ω. The purpose of the IF amplifier is to amplify the output waveform from the mixer. The first IF amplifier may be bypassed on the TRF6900.

3.4 Second IF Amplifier and Limiter [22]

The second IF amplifier has a typical gain of approximately 80 dB, and an input impedance of 330 Ω. A voltage level of 32 μV is required at terminal 39 (IF2_IN) to generate a limited signal at the limiter output. The output of the limiter is internally connected to the FM/FSK demodulator.

The limiter is internally connected to the output of the second IF amplifier. The function of the limiter circuit is to remove amplitude variations from the IF waveform. Amplitude variations in the IF waveform must be removed since the demodulator circuit responds to amplitude variations as well as frequency variations in the IF waveform. When the demodulator responds to amplitude variations, the receiver sensitivity is decreased and the distortion in the demodulated waveform is increased.

3.5 Received-Signal-Strength Indicator (RSSI) [22]

The received-signal-strength Indicator (RSSI) output voltage at terminal 33 (RSSI_OUT) is proportional to the RF limiter input level. The slope of the RSSI circuit is typically 19 mV/dB for a frequency range from 10 MHz to 21.4 MHz.

The received-signal-strength indicator is a summing network with inputs from the second IF amplifier and limiter circuits. This summing network produces a voltage which is used to indicate received-signal strength. The output voltage of the summing network is a logarithmic function of the received signal.

3.6 FM/FSK Demodulator [22] [6]

A quadrature-demodulator circuit is used, as shown in Figure 15.

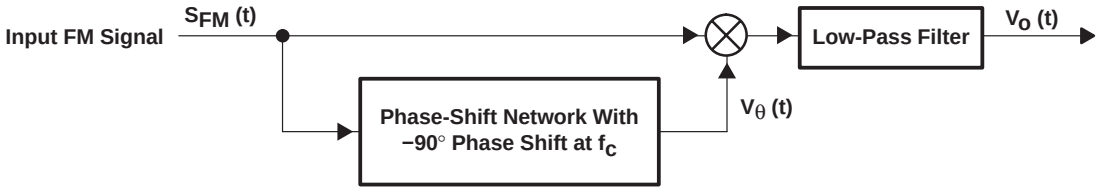


Figure 15. FM Demodulator Block Diagram

The phase-shift network is an external RLC-tank circuit. The low-pass filter amplifier/ post-detection amplifier performs the low-pass filter function.

3.6.1 Calculation of Components for the Demodulation-Tank Circuit for TRF6900

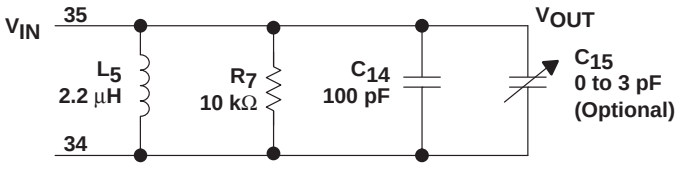


Figure 16. Demodulation Tank Circuit

The demodulation-tank circuit is shown in Figure 16. The bandwidth of the demodulation tank circuit must be greater than the bandwidth of the IF filters used. As a rule of thumb, the demodulation tank circuit bandwidth BW_t must be set to 1.5 times the IF filter bandwidth. The composite bandwidth of the IF filter or filters is determined in equation (23).

$$BW_{Comp} = \frac{1}{\sqrt{\left(\frac{1}{BW_1^2} + \frac{1}{BW_2^2}\right)}} \tag{23}$$

Where:

BW_{Comp}: Composite bandwidth of the IF filter(s)
BW_1: Bandwidth of the first IF filter
BW_2: Bandwidth of the second IF filter

NOTE: If only one IF filter is used, the composite bandwidth BW_{Comp} is equal to the single filter bandwidth.

The Q of the IF filters must then be determined:

$$Q_{IF} = \frac{f_c}{BW_{Comp}} \tag{24}$$

Where:

Q_{IF}: Q of the IF circuit
f_c: Center frequency of the IF chain
BW_{Comp}: Composite bandwidth of the IF filters

The quality factor Q_T of the demodulation tank circuit is equal to:

$$Q_T = \frac{f_c}{1.5 \times BW_{Comp}} \tag{25}$$

Where:

Q_T: Q of the demodulation-tank circuit
f_c: Center frequency of the IF chain
BW_{Comp}: Composite bandwidth of the IF filters

The quality factor Q_T of the demodulation tank circuit is also equal to:

$$Q_T = \frac{Q_{IF}}{1.5} \tag{26}$$

The inductor chosen for the demodulation tank circuit determines the quality factor of the demodulation tank circuit (Q_T), because inductors have low values of Q compared to capacitors. The inductor is chosen to have as high a value of Q as possible to properly resonate with the capacitor.

If the inductor chosen has a Q value higher than Q_{IF} (calculated from equation (26)), the Q of the demodulation tank circuit must be decreased. The addition of a resistor in parallel with the inductor decreases the Q of the demodulation-tank circuit (Q_T).

The procedure for decreasing the Q_T of the demodulation tank is as follows:

- Determine Q_{IF} using equations (23) and (24).
- Determine Q_T using equation (25) or (26).
- Use the following equations to choose an inductor and a capacitor to resonate at the proper IF frequency:

The IF frequency f_c is known. The value of the inductor L is chosen for a high Q value.

The resistive part of the inductor impedance is calculated using equation (27).

$$R_{ind} = Q_{ind} \times 2 \times \pi \times f_c \times L \tag{27}$$

Where:

R_{ind}: Resistive part of the inductor impedance
Q_{ind}: Q of the inductor
f_c: IF frequency
L: Value of the inductor

Capacitor C is then calculated using equation (28).

$$C = \frac{1}{4 \times \pi^2 \times f_c^2 \times L} \tag{28}$$

Where:

C: Value of the capacitor
f_c: IF frequency
L: Value of the inductor

The resistive part of the tank impedance R_{tank} is calculated using equation (29).

$$R_{tank} = Q_T \times 2 \times \pi \times f_c \times L \tag{29}$$

Where:

Q_T: Q of the demodulation-tank circuit
f_c: IF frequency
L: Value of the inductor

The resistor R_{ext} required to decrease the Q of the demodulator-tank circuit is calculated using equation (30).

$$R_{ext} = \frac{R_{ind} \times R_{tank}}{R_{ind} - R_{tank}} \tag{30}$$

The equivalent parallel resistance R_p of the tank circuit is calculated using equation (31).

$$R_P = \frac{R_{ind} \times R_{ext}}{R_{ind} + R_{ext}} \tag{31}$$

The Q of the demodulator tank circuit Q_T is verified by solving equation (32).

$$Q_T = \frac{R_P}{2 \times \pi \times f_c \times L} \tag{32}$$

Equation (33) is used to verify the bandwidth (BW) of the demodulator-tank circuit.

$$BW_t = \frac{f_c}{Q_T} \tag{33}$$

The following example is used to illustrate this procedure.

Example 2. Calculation of the Component Values for a Demodulation-Tank Circuit

Task:	Design an RLC network that implements an IF quadrature-FM-detector.	
Given:	IF frequency (f_c) = 10.7 MHz	
	IF bandwidth (BW_1) = 150 kHz	
Definitions:	f_c = 10.7 MHz	IF center frequency
	BW_1 = 150 kHz	Bandwidth of first IF filter
	BW_2 = not installed	Bandwidth of second IF filter

NOTE: Since the second IF filter is not installed, its bandwidth is considered to be infinite.

$Q = \frac{f_c}{BW}$ Definition of Q

$\omega_c = 2\pi f_c$ Definition of ω_c

BW_{Comp} is the composite bandwidth of the IF filter (or filters, if more than one IF filter is used). This bandwidth is 3 dB if the 3-dB bandwidth for each filter is used in the calculations. This bandwidth is determined in equation (34).

$$BW_{Comp} = \frac{1}{\sqrt{\left(\frac{1}{BW_1^2} + \frac{1}{BW_2^2}\right)}} \tag{34}$$

NOTE: If only one IF filter is used, the composite bandwidth BW_{Comp} is equal to the bandwidth of the single filter used.

$$BW_{Comp} = \frac{1}{\sqrt{\left(\frac{1}{(150\ kHz)^2}\right)}}$$

$$BW_{Comp} = 150\ kHz$$

The Q of the IF filter or filters should then be determined in equation (35).

$$Q_{IF} = \frac{f_c}{BW_{Comp}}$$

$$Q_{IF} = \frac{10.7\ MHz}{150\ kHz} \tag{35}$$

$$Q_{IF} = 71.333$$

The Q of the demodulation tank circuit Q_T is determined in equation (36).

$$Q_T = \frac{f_c}{1.5 \times BW_{Comp}}$$
$$Q_T = \frac{10.7\ MHz}{1.5 \times 150\ kHz} \quad (36)$$
$$Q_T = 47.556$$

The Q of the demodulation tank circuit Q_T can be determined in equation (37).

$$Q_T = \frac{Q_{IF}}{1.5}$$
$$Q_T = \frac{71.333}{1.5} \quad (37)$$
$$Q_T = 47.556$$

The IF frequency f_c is known. The value of the inductor L is chosen for a high-Q value.

$L = 2.2\ \mu H$ With a Q of approximately 78 (measured) for the inductor used.

$Q_{ind} = 78$ Measured value

NOTE: The inductor Q was measured using a Hewlett-Packard HP8753 vector network analyzer. The inductor is connected with one side to the center pin of an SMA PCB connector and the other side to the SMA connector ground. An S_{11} measurement is performed with the network analyzer displaying the result in Smith Chart format. Markers are placed at the frequencies of interest. The network analyzer provides a marker display of frequency, inductance, and R + jω, from which Q can be calculated. Q by definition is equal to jωL/R.

The resistive part of the inductor impedance is calculated in equation (38).

$$R_{ind} = Q_{ind} \times 2 \times \pi \times f_c \times L$$
$$R_{ind} = 78 \times 2 \times \pi \times 10.7\ MHz \times 2.2\ \mu H \quad (38)$$
$$R_{ind} = 11.537\ k\Omega$$

Capacitor C is then calculated using equation (39).

$$C = \frac{1}{4 \times \pi^2 \times f_c^2 \times L}$$
$$C = \frac{1}{4 \times \pi^2 \times (10.7\ MHz)^2 \times 2.2\ \mu H} \quad (39)$$
$$C = 100.566\ pF \sim 100\ pF\ (standard\ value)$$

The resistive part of the tank impedance R_{tank} is calculated using equation (40).

$$R_{tank} = Q_T \times 2 \times \pi \times f_c \times L$$
$$R_{tank} = 47.556 \times 2 \times \pi \times 10.7\ MHz \times 2.2\ \mu H \quad (40)$$
$$R_{tank} = 7.034\ k\Omega$$

The resistor R_{ext} required to decrease the Q of the demodulation tank circuit is calculated using equation (41).

$$R_{ext} = \frac{R_{ind} \times R_{tank}}{R_{ind} - R_{tank}}$$

$$R_{ext} = \frac{11.537\ k\Omega \times 7.034\ k\Omega}{11.537\ k\Omega - 7.034\ k\Omega} \quad (41)$$

$$R_{ext} = 18.021\ k\Omega \sim 20\ k\Omega \text{ (standard value)}$$

The equivalent parallel resistance R_p of the tank circuit is calculated in equation (42), using a standard value of 20 kΩ.

$$R_p = \frac{R_{ind} \times R_{ext}}{R_{ind} + R_{ext}}$$

$$R_p = \frac{11.537\ k\Omega \times 20\ k\Omega}{11.537\ k\Omega + 20\ k\Omega} \quad (42)$$

$$R_p = 7.316\ k\Omega$$

The Q of the demodulation-tank circuit Q_T is verified by solving equation (43).

$$Q_T = \frac{R_p}{2 \times \pi \times f_c \times L}$$

$$Q_T = \frac{7.316\ k\Omega}{2 \times \pi \times 10.7\ MHz \times 2.2\ \mu H} \quad (43)$$

$$Q_T = 49.463$$

Equation (44) is used to verify the bandwidth (BW) of the demodulator tank circuit.

$$BW_t = \frac{f_c}{Q_T}$$

$$BW_t = \frac{10.7\ MHz}{49.463} \quad (44)$$

$$BW_t = 216\ kHz$$

On the TRF9600 EVM, a 10-kΩ resistor is used to de-Q the tank. With a 10-kΩ resistor, Q_T is equal to 36.17 with an associated BW_t of 296 kHz. If an inductor with a lower Q value is used, a de-Qing resistor may not be needed.

3.7 Low-Pass Filter Amplifier/Post-Detection Amplifier

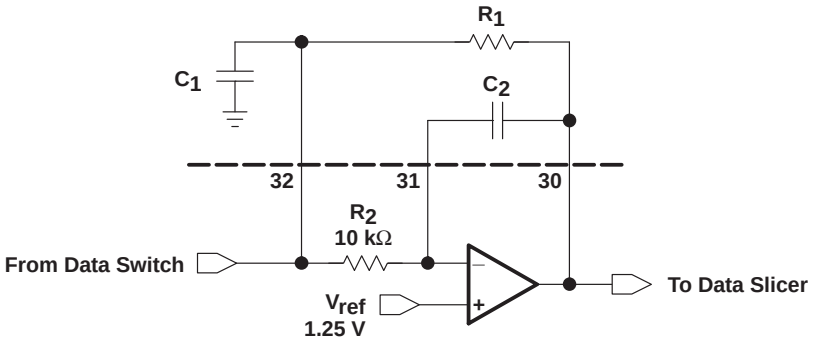


Figure 17. Low-Pass Filter Amplifier/Post-Detection Amplifier

The low-pass filter amplifier/post-detection amplifier is used to amplify the output of the demodulator circuit and to provide filtering of unwanted products from the demodulator circuit. The cutoff frequency, or –3-dB corner frequency, of the low-pass filter amplifier should be greater than two times the data rate.

The low-pass filter amplifier/post-detection amplifier is configured to operate as a current-to-voltage amplifier. The amplifier configuration shown in Figure 17 is a second order low-pass filter. The low-pass-filter bandwidth is determined by external components R_1, C_1, C_2, and internal resistor R_2. Internal resistor R_2 has a fixed value of 10 kΩ. An internal 10-pF capacitor sets the maximum –3-dB corner frequency to approximately 0.75 MHz.

The –3-dB corner frequency for a second-order low-pass filter is determined by equation (45).

$$f_c = \frac{1}{2\pi\sqrt{R_1 \times R_2 \times C_1 \times C_2}} \quad (45)$$

Where:

$C_1 \approx 3 \times C_2$

Resistor R_1 is set for maximum voltage gain. Laboratory measurements have shown that the maximum value of R_1 is 39 kΩ. The output voltage does not increase if resistor R_1 is increased above this maximum value.

Equation (46) is used to determine the voltage gain A.

$$A = \frac{R_1}{R_2} \quad (46)$$

Capacitor C_2 is determined by equation (47).

$$C_2 = \frac{1}{2 \times Q \times R_1 \times \omega_c} \quad (47)$$

Where:

ω_c: $2\pi f_c$
Q: Quality factor

This value of Q is determined from the transfer function of the low-pass filter amplifier/ post-detection amplifier. The classic form of this transfer function is:

$$H(s) = \frac{-h}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \quad (48)$$

Another form of the transfer function equation is:

$$H(s) = \frac{-h}{s^2 + 2\zeta\omega_o s + \omega_o^2},$$

where ζ is the damping factor.

When the two forms of the transfer function equation are compared, the relationship between Q and ζ is as shown in equation (49).

$$Q = \frac{1}{2\zeta} \quad (49)$$

Ringing and peaking are minimized if ζ is set to approximately 1.1 so that the filter circuit is overdamped. The required Q is determined to be approximately 0.45 using the relationship of equation (49).

The value of capacitor C_1 is determined by substitution of equation (46) (solved for R_2) into equation (47) (solved for C_1) to yield:

$$C_1 = \frac{A}{(\omega_c)^2 \times (R_1)^2 \times C_2} \quad (50)$$

Example 3 is used to demonstrate the calculation of the low-pass filter amplifier/post-detection amplifier values for the evaluation board.

The –3-dB cutoff frequency (f_c) for this example is 45 kHz. The f_c was chosen to be two times a data rate of 20 kHz (equal to a bit rate of 40 kbps), plus 5 kHz of margin to account for part tolerances, etc.

Example 3. Calculation of external circuit components for the low-pass filter amplifier/ post-detection amplifier.

Requirement: Determine the required values of external components R_1, C_1, and C_2 for a −3-dB cutoff frequency (f_c) of 45 kHz.

Given:

R_1 = 39 kΩ	Resistor R_1 is chosen for maximum voltage gain (A_v) of low-pass filter amplifier/post-detection amplifier.
R_2 = 10 kΩ	Resistor R_2 is an internal fixed resistor.
f_c= 45 kHz	Cutoff frequency chosen as 2 × data rate of 20 kHz, plus a 5 kHz margin.
ζ = 1.111	Damping factor, chosen to be greater than 1 to minimize peaking and overshoot.

Definitions:

$$\omega_c = 2\pi f_c \quad (51)$$

Calculations:

Calculate the voltage gain A_V:

$$A = \frac{R_1}{R_2} \tag{52}$$

$$A = \frac{39\ k\Omega}{10\ k\Omega}$$

$$A = 3.9$$

Calculate Q:

$$Q = \frac{1}{2\zeta} \tag{53}$$

$$Q = \frac{1}{2(1.111)}$$

$$Q = 0.45$$

Calculate ω_c:

$$\omega_c = 2\pi f_c \tag{54}$$

$$\omega_c = 2\pi(45\ kHz)$$

$$\omega_c = 2.8274 \times 10^5$$

Calculate Capacitor C_2:

$$C_2 = \frac{1}{2 \times Q \times R_1 \times \omega_c} \tag{55}$$

$$C_2 = \frac{1}{2 \times 0.45 \times 39\ k\Omega \times 2.8274 \times 10^5}$$

$$C_2 = 100.768\ pF$$

$C_2 = 100$ pF Nearest standard value

Calculate Capacitor C_1:

$$C_1 = \frac{A}{(\omega_c)^2 \times (R_1)^2 \times C_2} \tag{56}$$

$$C_1 = \frac{3.9}{(2.8274 \times 10^5)^2 \times (39\ k\Omega)^2 \times 100\ pF}$$

$$C_1 = 320.738\ pF$$

$C_1 = 330$ pF Nearest standard value

Check calculations:
Calculate the cutoff frequency using standard values for components:

$$f_c = \frac{1}{2\pi\sqrt{R_1 \times R_2 \times C_1 \times C_2}} \quad (57)$$

$$f_c = \frac{1}{2\pi\sqrt{39\ k\Omega \times 10\ k\Omega \times 330\ pF \times 100\ pF}}$$

$$f_c = 44.364\ kHz$$

Calculate Q using standard value for components:

$$Q = \frac{\sqrt{\left(\frac{C_1}{C_2} \times A\right)}}{2A} \quad (58)$$

$$Q = \frac{\sqrt{\left(\frac{300\ pF}{100\ pF} \times 3.9\right)}}{2(3.9)}$$

$$Q = 0.46$$

Calculate damping factor ζ using standard values for components:

$$Q = \frac{1}{2\zeta} \quad (59)$$

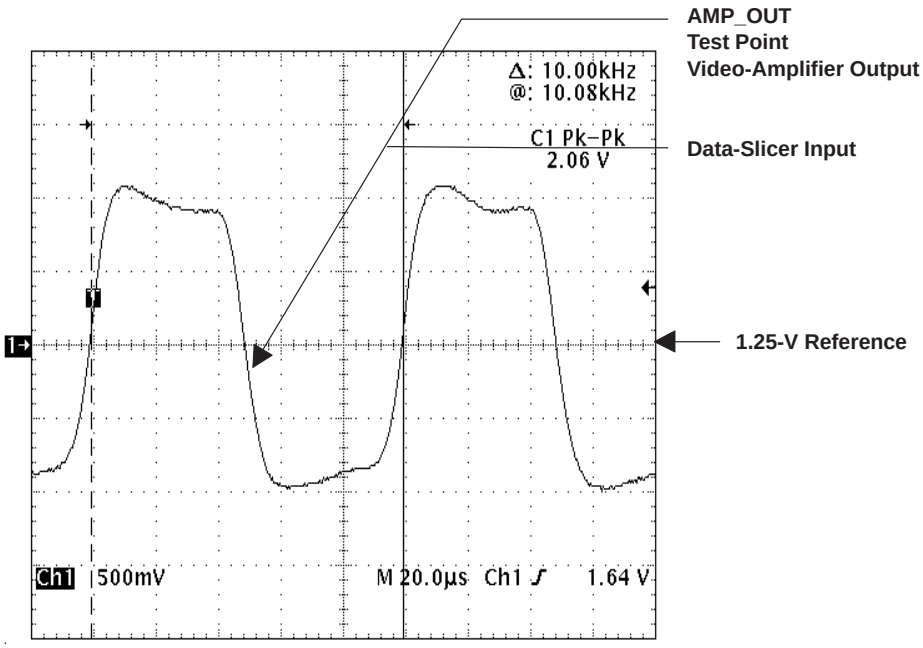
Therefore,

$$\zeta = \frac{1}{2Q}$$

$$\zeta = \frac{1}{2(0.46)}$$

$$\zeta = 1.087$$

Figure 18 shows the output waveform of the low-pass filter amplifier/post-detection amplifier. The output of the amplifier is centered at 1.25 V, the reference voltage.



NOTE: Figure 17, the low-pass filter amplifier/post-detection amplifier schematic, has a connection to V_{ref} as an input to the + terminal of the amplifier. Therefore, the low-pass filter amplifier/post-detection amplifier output is symmetrical about 1.25 V.

Figure 18. Low-Pass Filter Amplifier/Post-Detection Amplifier Output Waveform

3.8 Data Slicer [22]

The data slicer is a comparator circuit which outputs the necessary binary-logic levels for external CMOS circuitry. The output of the data slicer is the demodulated data at CMOS levels.

The block diagram shown in Figure 19 details the automatic-frequency-control (AFC) loop used to determine the data slicer decision threshold.

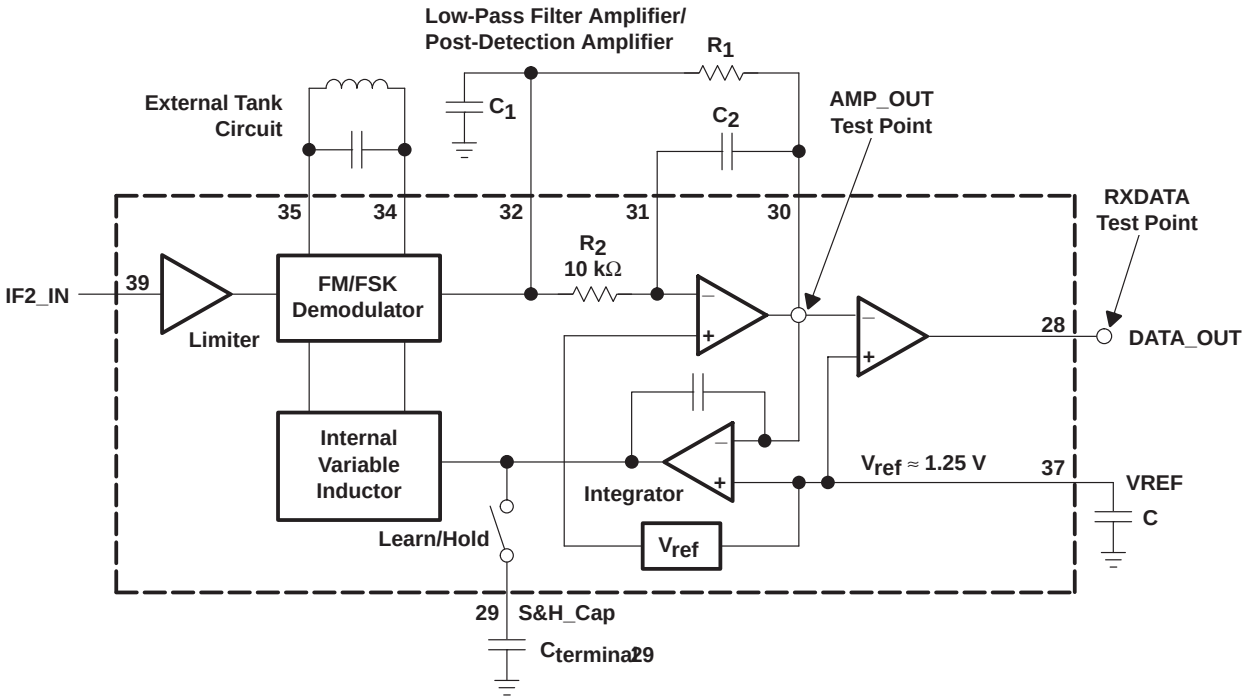


Figure 19. AFC Control Loop Block Diagram

Figure 20 shows the input and output of the data slicer.

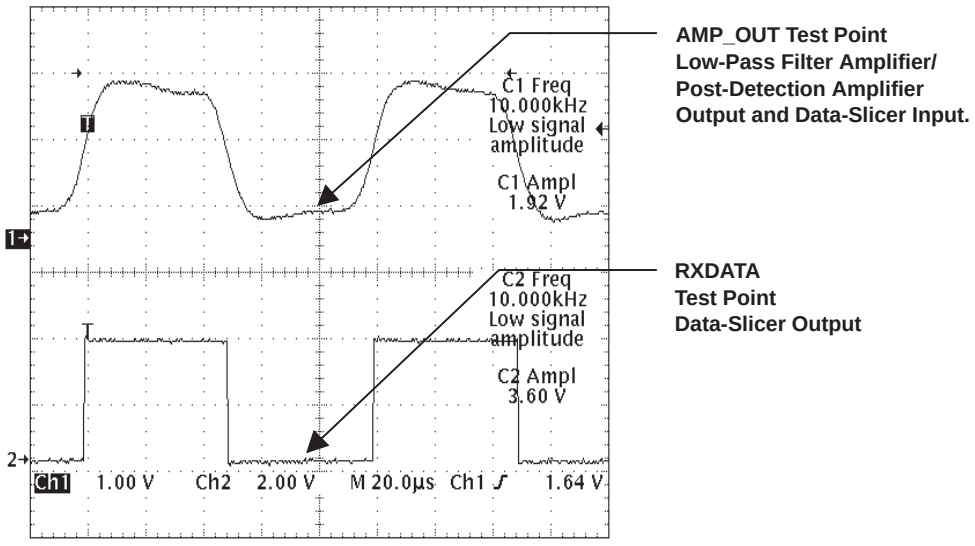


Figure 20. Data Output at AMP_OUT and RX_DATA Test Points

A typical input from the low-pass filter amplifier/post-detection amplifier to the data slicer is shown in the upper trace of Figure 20. The Amp_Out test point shown in Figure 19 is symmetrical at about 1.25 V (the reference voltage V_{ref} of 1.25 V determines the decision threshold of the data slicer). The data slicer output measured at the RXDATA test point is shown in the lower trace of Figure 20. The amplitude of the waveform at the Amp_Out test point is determined by the gain of the low-pass filter amplifier/post-detection amplifier.

The integrator is an error amplifier which takes as an input the filtered output from the low-pass filter amplifier/post-detection amplifier. The integrator generates an error voltage proportional to the difference between the frequency error of the external-tank circuit and the second IF amplifier/limiter output signal. The error voltage output of the integrator adjusts the value of the internal variable inductor, providing a fine-tune adjustment to the external tank circuit.

The time constant of the AFC loop, used during learning mode, is calculated using the following equation:

$$\tau_{AFC} = 22\ k\Omega \times C_{terminal\ 29} \quad (60)$$

The 22-kΩ resistor in equation (60) is internal to the TRF6900. The sample-and-hold (S&H) capacitor connected to terminal 29 is the only variable in equation (60) that can be used to adjust τ_{AFC}.

The AFC controls the resonant frequency of the external LC-tank circuit only in the learn mode. The AFC is open when the hold mode is selected. The S & H capacitor is charged during the learn mode; this capacitor provides the dc-threshold offset voltage (offset from 1.25 V) to the data slicer during the hold mode. An in-depth discussion of the learn and hold modes and the AFC loop is provided in the next section.

3.9 Learn and Hold Mode

The TRF6900 data slicer provides a binary-logic-level signal at the DATA_OUT terminal. This signal is derived from the demodulated and low-pass-filtered, received RF signal. A decision threshold for the data slicer, V_{ref}, must be maintained to distinguish a received 1 from a received 0 properly and to minimize any bit errors. This decision threshold is always set to 1.25 V, however, a dc offset is introduced to ensure a proper decision in the presence of a nonconstant-dc bit sequence during receive.

As part of the AFC loop, the data slicer constantly integrates the incoming signal when in the learn mode and charges external capacitor $C_{terminal\ 29}$ to an offset voltage from the dc voltage level V_{ref}, which is proportional to the average demodulation dc-level. This dc voltage level (V_{ref} together with the offset voltage) is used as the decision threshold. The offset voltage is controlled by the internal regulation loop and can be measured at terminal 29. While in the learn mode, $C_{terminal\ 29}$ determines the integration time constant τ_{AFC} of the entire AFC loop.

You can continually operate the TRF6900 receiver in learn mode if the TRF6900 is receiving a constant dc (also called dc free) code such as Manchester, RZ, or biphase. However, a brief training or learning sequence is required at the beginning of each transmitted data packet to ensure that the external capacitor on the receiver is charged to the correct dc threshold.

The training sequence must be constant-dc. Therefore, the use of alternating 1s and 0s is recommended for this sequence. An alternating training sequence of 1s and 0s exhibits constant dc, independent of the data coding scheme used.

If the device is kept in learn mode and is receiving a nonconstant-dc code (such as NRZ) during reception of valid data, the decision level is altered by long 1 or 0 sequences. Therefore, if a nonconstant-dc data coding scheme is used, you must periodically switch between learn and hold modes.

While in hold mode, the internal regulation loop is open and an external dc offset can be applied to terminal 29 to introduce an equivalent offset for proper 0 or 1 decisions.

When using nonconstant-dc codes, the unit is switched to the hold mode for reception of valid data after the training sequence. The data slicer stops integrating and uses the voltage V_{ref} in conjunction with the offset voltage stored on $C_{terminal\ 29}$ as the decision threshold. Since the charge on the external capacitor deteriorates, it must be periodically recharged to the average dc level of the received data for proper data slicing. Thus, the unit must go back to learn mode, receive a training sequence to charge the external capacitor, set to hold mode, receive valid data, and so on.

The value of the external capacitor and the duration of the training sequence are governed by equations (60) and (61), respectively.

As a rule of thumb, the time constant τ_{AFC} (equal to 22 kΩ x $C_{terminal\ 29}$) of the AFC loop must be at least five times greater than the baseband modulating signal's fundamental period T_{fund}.

$$5 \times T_{fund} = 22\ k\Omega \times C_{terminal\ 29} \quad (61)$$

With T_{fund} known, equation (61) is solved for $C_{terminal\ 29}$

NOTES:

1. For nonconstant-dc codes:

   For NRZ, the maximum fundamental frequency of the baseband modulating waveform, F_{fund}, is $1/2T_b$ => $T_{fund} = 2T_b = T_o$. The advantage of using nonconstant dc codes is that the system uses half the bandwidth to transmit the same data rate as compared to constant-dc codes. A disadvantage is that you need to switch between learn and hold modes on the TRF6900; that is, the TRF6900 device requires a periodic training sequence while in learn mode, followed by a switch to hold mode for reception of each data packet.

2. For constant-dc codes:

   For Manchester, the maximum fundamental frequency of the baseband modulating waveform, F_{fund}, is $1/T_b$ => $T_{fund} = T_b = T_o/2$. The disadvantage of using constant-dc codes is that you need to use two times the bandwidth required with NRZ to get the same data rate. The advantage is that you do not need to switch between learn and hold modes on the TRF6900. You must initially account for the charge-up of $C_{terminal\ 29}$ when coming out of standby mode, and periodically redo the learning sequence at the beginning of each data packet. However, you can keep the TRF6900 device in learn mode continuously.

3. T_b = 1/bit rate
   T_o = 1/data rate = 2/bit rate
   $2T_b = T_o$
   data rate = $1/T_o = 1/2T_b$ [Hz]
   bit rate = R = $1/T_b$ [bps]
   (See Figure 25)

As a first approximation of the duration of the learning sequence, which includes a guard band for manufacturing tolerances and other factors, it is recommended to make the duration two times the minimum required.

Duration of training sequence = $2 \times 5 \times \tau_{AFC} = 10 \times \tau_{AFC}$

$$= 10 \times 22\ k\Omega \times C_{terminal\ 29} \quad (62)$$

For example:

(1) Nonconstant-dc coded data (NRZ):
Bit rate = 10 kbps, F_{fund} = 5 kHz => T_{fund} = 200 µs
BW required = B
τ_{AFC} = 22 kΩ x $C_{terminal\ 29}$
5 x 200 µs = 1000 µs = 22 kΩ x $C_{terminal\ 29}$, solve for $C_{terminal\ 29}$:
$C_{terminal\ 29} \approx 46$ nF
For a guard band, the alternating 1 and 0 learn sequence duration must be:
$10 \times \tau_{AFC} = 10 \times 200$ µs = 2 ms

(2) Constant dc coded data (Manchester, RZ, and biphase):
Bit rate = 10 kbps, F_{fund} = 10 kHz => T_{fund} = 100 µs
BW required = 2B
τ_{AFC} = 22 kΩ x $C_{terminal\ 29}$
5 x 100 µs = 500 µs = 22 kΩ x $C_{terminal\ 29}$, solve for $C_{terminal\ 29}$:
$C_{terminal\ 29} \approx 23$ nF
For a guard band, the alternating 1 and 0 learn sequence duration must be:
$10 \times \tau_{AFC} = 10 \times 100$ µs = 1 ms

These first approximations to the length of the learning sequence are a good starting point and may be optimized (reduced) at a later time based on field test results.

Note that a very fast data rate can be used for the learning sequence, followed by a lower data rate for data transmission. This allows for a short learning sequence time in the receiver, a technique patented by Texas Instruments. A slightly larger capacitor takes longer to charge (longer learning sequence duration), but the charge lasts longer and does not need to be re-learned as often. Conversely, a smaller capacitor takes a shorter time to charge (shorter learning sequence), but the charge does not last long and must be relearned more often.

The external capacitor holds the charge used for the decision threshold for several seconds. However, the capacitor is discharged much faster if the device is set to standby mode, or if the data slicer/demodulator is disabled.

The following sequence of events, in conjunction with Figure 21, can be used to better illustrate the use of the learning sequence and the learn and hold modes in a typical application:

1. Transmitter (TX) is transmitting a learning sequence of alternating 1s and 0s.
2. Receiver (RX) is put into active mode from standby mode: PLL, DDS, VCO, and DEMOD all start to power up and activate. RX is also put into learning mode.
3. $C_{terminal\ 29}$ starts to charge up almost immediately.
4. TX continues to transmit a learning sequence.
5. After 600 µs (approximately 1 ms), the RX puts out data—not necessarily valid data. This 1 ms is mostly a function of the start-up properties of the PLL, DDS, VCO, DEMOD, and the integration time constant of the entire AFC loop. More learning sequences for a guard band, followed by a start preamble are needed.
6. Approximately 1 ms of additional learning sequence is used. Note that a portion of the total learning sequence duration needed, as per equation (62), is accounted for during the

initial RX start-up time. The remainder of the total time is needed to secure proper reception and to give the microcontroller enough time to recognize the learning sequence and look for a start preamble.

7. TX outputs a start preamble or a START bit.
8. RX receives a start preamble or START bit that TX produces, and determines that learning is over and data is to follow. RX switches to hold mode.
9. TX outputs data in NRZ format.
10. RX receives valid data in hold mode.
11. TX outputs a stop preamble at the end of the data packet.
12. After reception of the data packet and stop preamble, RX returns to standby mode.
13. After a predetermined time, RX starts to output a learning sequence and the receiver is returned to active mode for reception. This sequence is repeated for the transmission and reception of each data packet.

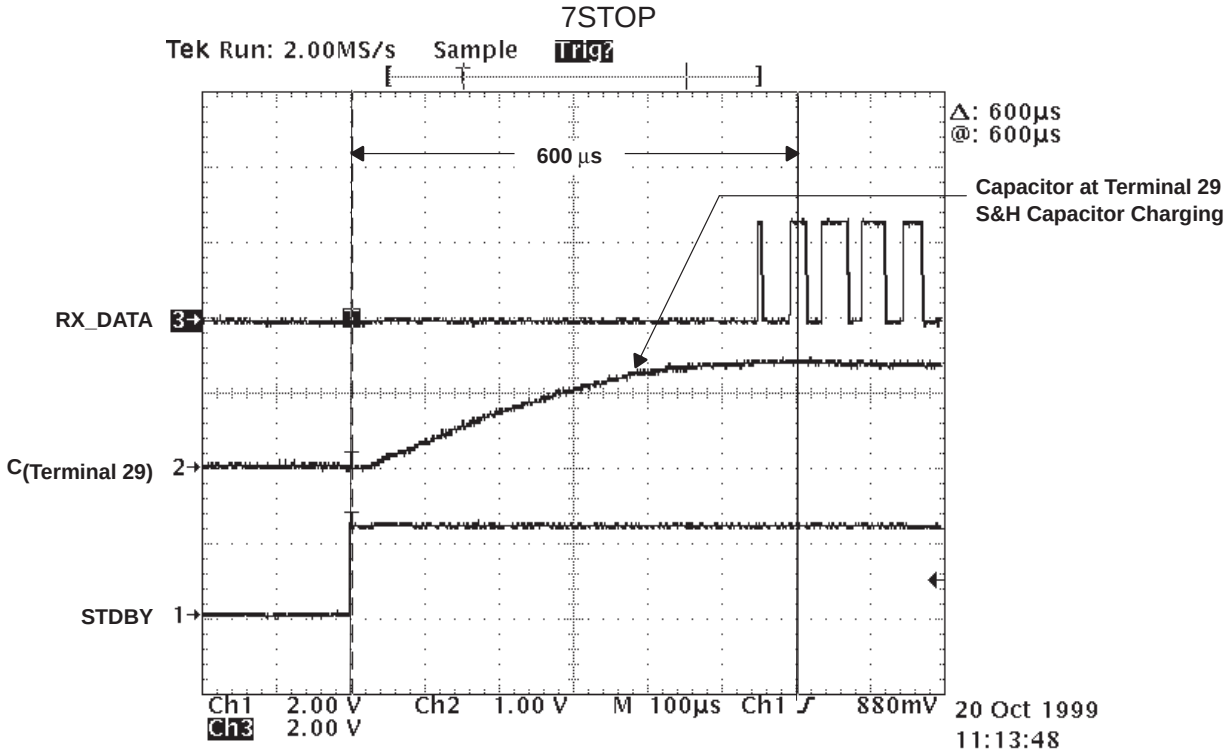


Figure 21. TRF6900 Wake-Up and Reception of Data

4 PCM-Data Coding Methods

Table 3. PCM Binary Coding Methods

PCM Code Type	RZ	NRZ	Phase Encoded	Ref. Level	Transitions
Unipolar RZ	X			0 level	Change of state from 0 to 1, and a 1 at 1/2-bit period

Unipolar NRZ		X		0 level	Change of state from 0 to 1 or from 1 to 0
NRZ-L (Level)		X		Center of pulse	Change of state from 0 to 1 or from 1 to 0
NRZ-M (Mark)		X		Center of pulse	1 or mark is represented by change in level, 0 or space is represented by no change in level
NRZ-S (Space)		X		Center of pulse	0 or space is represented by change in level, 1 or mark is represented by no change in level
Bi-ϕ-Level, Manchester			X	Center of pulse	A 1 is represented by a 1/2-bit pulse at the start of the bit interval. A 0 is represented by a 1/2-bit pulse at the end of the bit interval.
Bi-ϕ-Mark (Mark)			X	Center of pulse	Transition occurs at the beginning of each bit interval. 1 is represented by a second transition 1/2-bit later. 0 is represented by no second transition 1/2-bit later.
Bi-ϕ-Space (Space)			X	Center of pulse	Transition occurs at the beginning of each bit interval. 0 is represented by a second transition 1/2-bit later. 1 is represented by no second transition 1/2-bit later.

Coding methods such as Unipolar RZ, Unipolar NRZ, NRZ-L, NRZ-M, and NRZ-S require a learn mode training sequence. During this training sequence (alternate 1s and 0s), the TRF6900 receiver is operated in the learn mode. A switch to *hold* mode takes place after completion of the training sequence.

When continuous operation in the learn mode takes place using nonconstant dc codes such as Unipolar RZ, Unipolar NRZ, NRZ-L, NRZ-M, and NRZ-S, the decision level (that is, the dc level) is changed by the use of long 1 or 0 sequences.

The TRF6900 can be operated continuously in the learn mode when using constant dc codes or codes that have no dc component, such as Manchester, split-phase, bipolar RZ, and RZ−AMI codes. The RZ and split-phase codes assure at least one zero crossing per bit interval. However, the RZ and split-phase codes also require twice the transmission bandwidth of an NRZ code.

The split-phase codes are generated by multiplying an NRZ code by a square wave clock waveform with a period equal to the bit duration T_b.

4.1 PCM Code Waveforms

The various PCM waveforms are illustrated in Figure 22 and described Table 3.

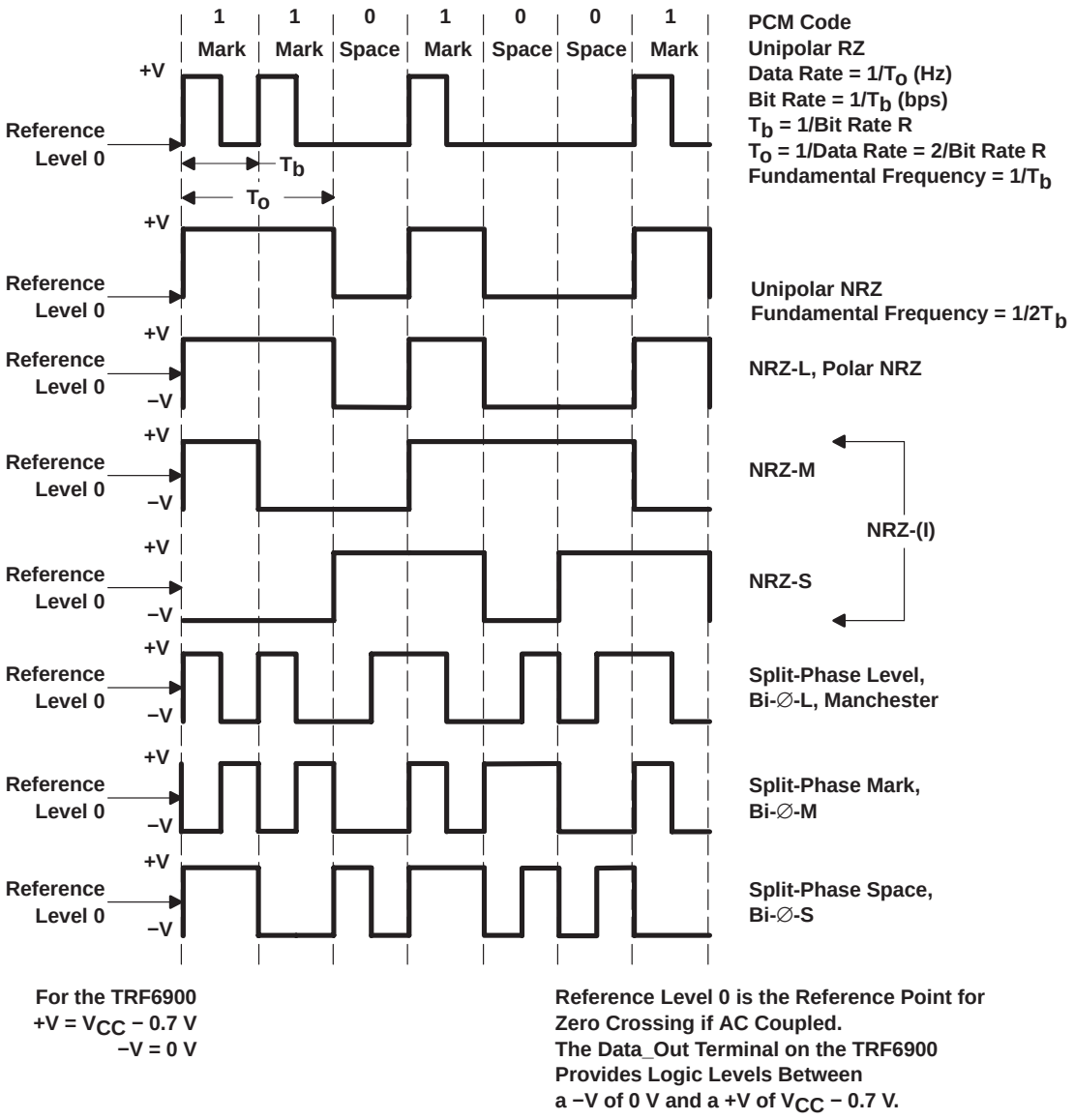


Figure 22. Pulse-Code-Modulation (PCM) Waveforms

5 Image Response

The use of a low IF frequency in the US ISM band (902 to 928 MHz) requires the proper system-architecture design. With the use of a 10.7-MHz IF, the image band and required LO band fall within the desired RF input band, as shown in Figure 23. Image noise from the receiver antenna, device LNA, and mixer-driver amplifiers may have an adverse effect on receiver sensitivity.

With a portion of the required LO in the desired input band, the LO phase noise, and the LO harmonics can remix in the mixer and cause further degradation of the receiver sensitivity.

With a 10.7-MHz IF, the image response of the mixer is 21.4 MHz away from the received signal. Due to the 26-MHz width of the ISM band, the image frequency is in-band for some portion of the band and cannot be filtered out with a fixed preselector filter.

Proper system architecture includes using only a portion of the ISM band and using a preselector filter that covers only the sub-band in use. In addition, it is important to ensure that the power of the desired signal is higher than any potential interferer when maximizing system sensitivity.

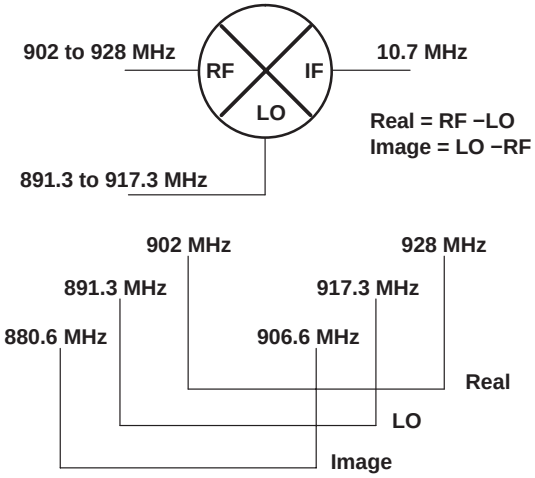


Figure 23. USA ISM Band Real vs Image Frequencies

6 Determination of Signal-to-Noise Ratio

The voltage level at the output of the low-pass filter amplifier/post-detection amplifier is the output signal-to-noise ratio (S/N). The output signal-to-noise ratio is usually expressed in decibels (dB). Equation (63) demonstrates how to determine the output S/N.

$$S/N = (C/N) + MNI \text{ dB} \tag{63}$$

Where:

S/N: Output signal-to-noise ratio, in dB
C/N: Input to the receiver carrier-to-noise ratio, in dB
MNI: Modulation-noise-improvement factor, in dB

The carrier-to-noise ratio (C/N) is the level of the input to the limiter stage. The carrier-to-noise ratio is calculated using equation (64).

$$C/N = -174 \text{ dB} + NF + 10 \times \log\left(BW_{IF}\right) + \text{RF Input Level (dB)} \tag{64}$$

Where:

–174 dB: Thermal noise floor
NF: Cascaded noise figure of the receiver system determined by the Friis equation [see equation (65)]
$BW_{IF:}$ IF filter bandwidth
RF Input Level: Minimum input signal level to the receiver (dB)

$$NF = NF_1 + \frac{NF_2 - 1}{Gain_1} + \frac{NF_3 - 1}{Gain_2 \times Gain_1} + \frac{NF_4 - 1}{Gain_3 \times Gain_2 \times Gain_1} + \ldots \tag{65}$$

Where:

$NF_n = 10^{NF_n(dB)/10}$
$Gain_n = 10^{Gain_n(dB)/10}$

$$MNI = \frac{3 \times m^2 \times BW_{IF}}{2 \times b} \quad (66)$$

$$MNI_{dB} = 10 \times \log MNI \quad (67)$$

Where:

MNI:	Modulation-noise-improvement factor.
m = Δf/b:	Modulation index
Δf:	Peak frequency deviation of the received signal
BW_{IF}:	IF filter bandwidth
b:	Bandwidth of the low-pass filter amplifier/post-detection amplifier. Bandwidth b is set to two times the data rate.

7 PCB-Board Layout Guidelines [20]

TI suggests the following layout guidelines to attain the most robust and functional PCB layout:

- The power amplifier output inductor must be placed as close as possible to the TRF6900 IC.
- The power amplifier, LNA, PLL, DDS, and demodulator V_{CC} bypass capacitors must be placed as close as possible to the TRF6900 IC.
- The VCO tank inductor must be placed as close as possible to the TRF6900 IC.
- The VCO tank capacitors must be placed as close as possible the VCO tank inductor. The traces from the VCO inductor to the VCO capacitors must be symmetrical.
- The LNA input-matching inductor must be placed as close as possible to the TRF6900 IC.
- The LNA matching-circuit components must be placed as close together as possible.
- The PLL loop filter traces must be kept as short as possible, and the ground plane must be used to isolate the PLL loop filter from the power amplifier output.
- The demodulation tank circuit inductor must be placed as close as possible to the TRF6900 IC.
- The demodulation tank circuit capacitors must be placed as close as possible to the demodulation tank inductor.
- Good grounding practices must be followed in the VCO, power amplifier, LNA input and output, IF, and crystal circuit areas.
- The PCB must ideally have one layer as a reference-ground plane. Any critical ground areas on the component side of the PCB should be connected by vias to this ground plane.
- The edges of the PCB board must be part of the ground plane.
- RF and digital grounds may be kept separate and tied at a common point.
- Ground vias must be spaced by a maximum of 1/4 wavelength of the highest frequency used. Closer spacing of the vias is recommended.

7.1 Clock-Circuit PCB-Layout Considerations

Layout considerations for the clock oscillator include:

- Keep short trace lengths between components.
- Eliminate parallel traces.
- Separate components to reduce coupling between component bodies.
- Use a ground plane to isolate signal paths.

8 FSK-Modulation Theory [1] [2] [3] [4] [7] [23]

Frequency-shift keying (FSK), as illustrated in Figure 24, is the modulation of a carrier signal by switching between two (or more) frequencies in response to baseband data. The TRF6900 uses continuous-phase FSK.

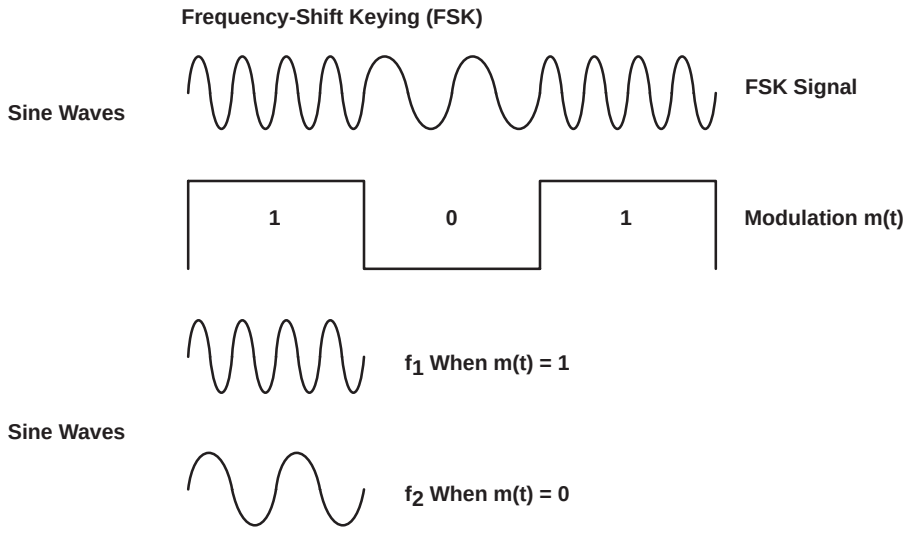


Figure 24. FSK-Modulated Output Signal vs Modulating Signal m(t)

The FSK signal is mathematically represented by equations (68) through (71).

$$s(t) = A_c \times \cos\left(\omega_c t + k_f \times \int_{-\infty}^{t} m(\alpha)d\alpha\right) \quad (68)$$

Or

$$s(t) = A \times \mathrm{Re}\left(g(t)e^{j\omega_c t}\right) \quad (69)$$

Where:

$$g(t) = A_c e^{j\theta(t)} \quad (70)$$

$$\theta(t) = k_f \times \int_{-\infty}^{t} m(\alpha)d\alpha \quad (71)$$

k_f: Frequency modulation gain constant (frequency deviation constant expressed in radians per second per unit of m(t)). Typical units for k_f are radians per second

per volt.
$k_{f:}$ Equal to $2\pi f_{d,}$ where f_d is the deviation constant in hertz per unit of m(t).
α: Integration dummy variable
$\theta(t)$: Phase waveform

The baseband signal is represented by m(t). This signal is discontinuous at switching time, but the phase function $\theta(t)$ is continuous, since it is proportional to the integral of m(t). If the data-input waveform is binary, the resulting FSK waveform is called binary FSK (BFSK).

Frequency-shift keying is a form of frequency modulation (FM). Frequency modulation is, in turn, a form of angle modulation. Therefore, the equations and theory that apply to FM modulation can be applied to FSK modulation. FM modulation requires that the time derivative of the phase of the carrier signal be varied linearly with the message signal m(t). The instantaneous frequency ω_i is defined in equations (72) through (74).

$$\omega_i(t) = \frac{d\theta_i}{dt} \tag{72}$$

$$\omega_i(t) = \omega_c + \frac{d\theta}{dt} \tag{73}$$

$$\frac{d\theta}{dt} = k_f m(t) \tag{74}$$

Where the function $\frac{d\theta}{dt}$ is the frequency deviation.

These equations show that the frequency deviation of the carrier is proportional to the modulating signal.

The output of the FM modulator is shown in equation (75).

$$s(t) = A_c \times \cos\left(\omega_c t + k_f \times \int_{-\infty}^{t} m(\alpha)d\alpha\right) \tag{75}$$

Substituting $k_f = 2\pi f_d$ into equation (75) yields:

$$s(t) = A_c \times \cos\left(\omega_c t + 2\pi f_d \times \int_{-\infty}^{t} m(\alpha)d\alpha\right) \tag{76}$$

The frequency deviation of the FM modulator is proportional to m(t). The instantaneous frequency of the FM modulator output is maximum when m(t) is maximum, and minimum when m(t) is minimum. Let m(t) = a cos $\omega_m t$, and substitute this value in equations (73) and (74).

$$\omega_i = \omega_c + a\,k_f \cos \omega_m t \tag{77}$$

With $\Delta\omega = a\,k_{f,}$ then

$$\omega_i = \omega_c + \Delta\omega \cos \omega_m t \tag{78}$$

The peak-frequency-deviation constant is defined as $\Delta\omega$.
Note: $\Delta\omega/2\pi = f_d = \Delta f$, and $\omega_m/2\pi = f_m$

The phase of the FM signal can then be defined as

$$\theta(t) = \omega_c t + (\Delta\omega/\omega_m)\sin\ \omega_m t \tag{79}$$

or

$$\theta(t) = \omega_c t + \beta \sin\ \omega_m t \tag{80}$$

Where β is the modulation index

$$\beta = \Delta\omega/\omega_m \qquad \beta = \Delta f/f_m \tag{81}$$

The modulation index β is only defined for sinusoidal modulation. When an arbitrary m(t) is used, the accepted expression for bandwidth uses the deviation ratio D.

D is defined as: $D = \dfrac{\text{peak frequency deviation}}{\text{Bandwidth of m(t)}}$; $D = (\Delta f/f_m)$, where f_m is the bandwidth of m(t)

The deviation ratio D performs the same function for nonsinusoidal modulation as the modulation index β performs for sinusoidal modulation.

If $\beta < 0.2$, the modulation is narrowband frequency modulation (NBFM). If $\beta > 0.2$, then the modulation is wideband frequency modulation (WBFM). For FSK, in most cases, the modulation is WBFM. The transmission bandwidth required for WBFM and/or FSK is determined by Carson's rule, equation (84).

You can define the modulation index and observe the FSK spectrum as the modulation index is varied. The frequency modulation index is defined in equation (82).

$$\text{Frequency modulation index } \beta = \frac{\Delta f}{B} \tag{82}$$

This index is for FM modulation with sinusoidal modulation, where Δf is the peak-frequency deviation and *B* is the bandwidth of the modulating signal. An alternate definition of the modulation index is sometimes used with digital signals—the digital modulation index, which is denoted by h.

$$\text{Digital modulation index} = h = \Delta f \times T_o = \frac{2\Delta f}{R} \tag{83}$$

Where:

$R = 1/T_b = 2/T_o$: Bit rate [bps]
T_b: Time interval for one bit
T_o: Period of the data modulation = 1/data rate [Hz]

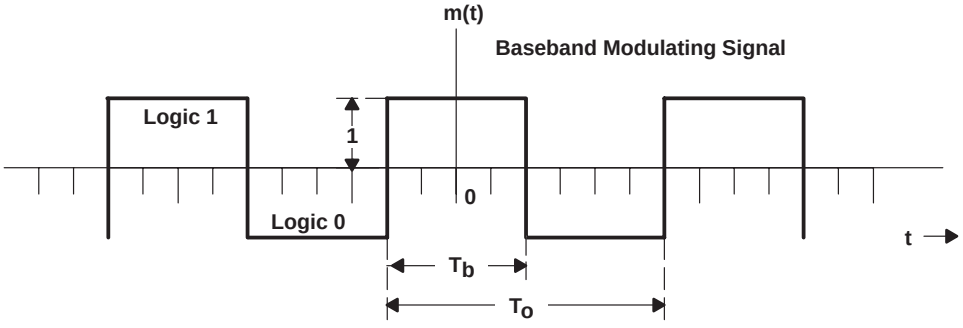


Figure 25. Input-Data Signal

Figure 25 illustrates the relationship between T_b and T_o. Figure 26 illustrates the FSK spectra as the modulation index h is varied from 0.5 to more than 1.5.

Depending on the modulation index of the signal, an FSK spectrum can appear (with pseudorandom data) anywhere between a single peak at the carrier and two peaks separated from the carrier. The separation of the peaks is not necessarily the frequency deviation. The distance between the peaks is a function of both the modulation index h and the frequency deviation.

When non-pseudorandom data is used, the output spectrum appears as two SINC functions that are composed of impulses. A non-pseudorandom data stream is an alternating 1,0,1,0,1,0… pattern. When the modulation index is varied, the two SINC functions get closer together or move further apart. When the modulation index h is increased from 0.5 to 1.0, the spectrum concentrates about f_1 and f_2. When the modulation index is increased beyond 2, the spectrum starts to spread out and the amplitude level decreases.

The modulation index h must be between 0.5 and 1 or 2 maximum to conserve bandwidth and minimize BER. Table 4 summarizes the modulation index information.

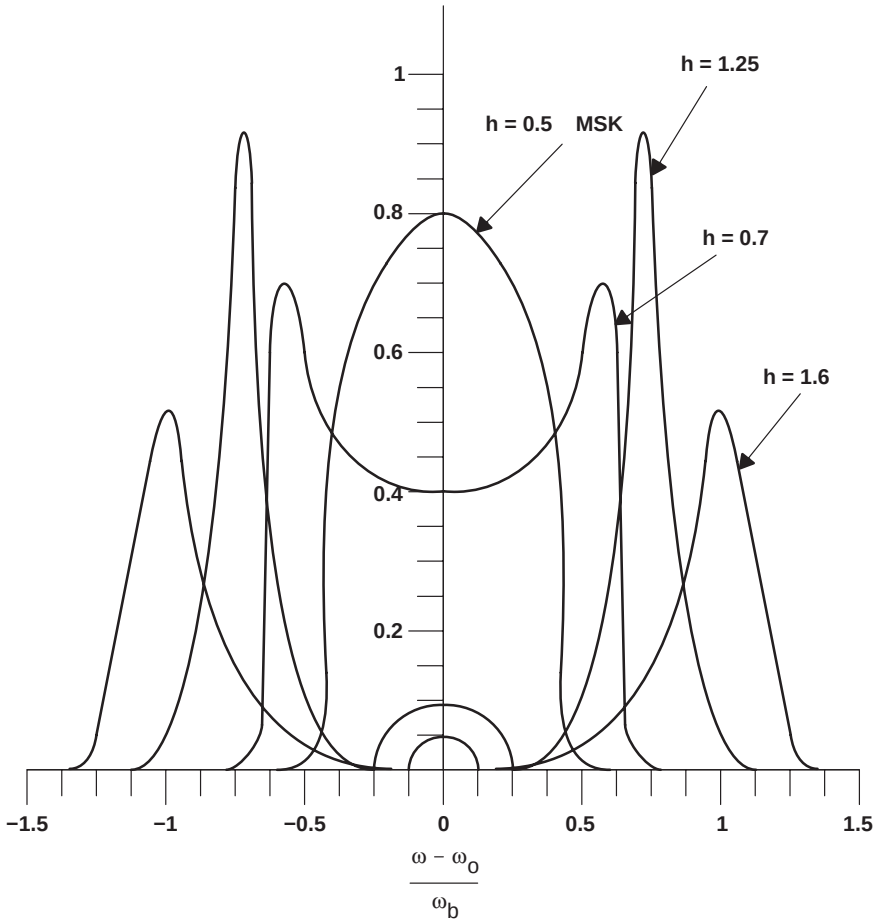


Figure 26. Power Spectral Density of FSK for Pseudorandom Data

Table 4. Modulation Index h vs Power Spectra

Modulation Index h	Power Spectra Effects
h < 0.5	FSK signals are less orthogonal and BER increases (do not use).
h = 0.5	Minimum shift keying. MSK equals the narrowest spectrum for orthogonality.
h ≈ 0.6	Spectrum is smooth and single-peaked at carrier frequency.
0.6 < h < 1.0	Spectrum is smooth and well confined; spectrum moves form single-peak at carrier frequency to peaks at M frequencies (as h -> 1, spectra begins to peak at M frequencies).
h = 1.0	Impulses occur at M frequencies.
h > 1.0	Spectrum is broadest, peaks outside carrier frequency ± bit rate/2, decreases in sharpness and amplitude.

9 Required Bandwidth for Transmit and Receive

The approximate bandwidth B_T for an FSK signal is given by Carson's rule shown in equation (84).

$$B_T = 2(\beta + 1)B \tag{84}$$

Where:
- β: Modulation index h
- B: Bandwidth of the modulation waveform, m(t); $B = 1/T_0$

When rectangular pulses are used (B = R), Carson's rule is stated as:

$$B_T = 2(\Delta f + R) \tag{85}$$

Where:
- B_T: Transmission bandwidth for the FSK signal
- Δf: Peak frequency deviation
- R: Bit rate

For wideband FSK (WBFSK) where $\beta > 1$, Δf is the dominant term and equation (85) can be reduced to:

$$B_T \cong 2\Delta f \text{ for WBFSK} \tag{86}$$

For narrowband FSK (NBFSK), where $\beta < 0.2$, the transmission bandwidth is found as:

$$B_T \cong 2B \cong 2R \text{ for NBFSK} \tag{87}$$

The bandwidth determined by equation (85) is generous and can be considered as the maximum bandwidth required. The minimum bandwidth required is bounded by:

$$B_T \cong 2\Delta f \text{ for WBFSK.} \tag{88}$$

Note: A periodic random data requires less bandwidth than periodic data.

Example 4.

Given an FSK system with the following parameters:

$f_d = \Delta f$ = 10-kHz peak deviation (20-kHz peak-to-peak frequency deviation)

$$\text{Bit rate } R = \frac{1}{T_b} = 10 \text{ kbps} \tag{89}$$

Bit duration = 1/10 kbps

Determine:

1. Digital modulation index h
2. Required bandwidth

Solution:

1. Digital modulation index h

$$\text{Digital modulation index} = h = \Delta f \times T_o = \frac{2\Delta f}{R}$$
$$\text{Digital modulation index} = h = 10\ \text{kHz} \times 200\ \mu\text{s} = \frac{2(10\ \text{kHz})}{10\ \text{kHz}} = 2 \quad (90)$$

2. Required bandwidth

   Carson's rule is stated as:

$$B_T = 2(\Delta f + R) \quad (91)$$

   Where:
   B_T: Transmission bandwidth for the FSK signal
   Δf: Peak frequency deviation
   R: Bit rate

$$B_T = 2(10\ \text{kHz} + 10\ \text{kHz})$$
$$B_T = 40\ \text{kHz} \quad (92)$$

   As a lower bound for WBFSK,

   $B_T \cong 2\Delta f \cong 2(10\ \text{kHz}) \cong 20\ \text{kHz}$

   Therefore, a minimum bandwidth of 20 kHz is required for this system, with a maximum bandwidth of 40 kHz as the upper bound.

10 Bit Error Rate

For noncoherent FSK modulation the bit error rate (BER) is defined in equation (93).

$$P_e = \frac{1}{2} e^{-\frac{1}{2} \times \left(\frac{E_b}{N_o}\right)} \quad (93)$$

Where:
P_e: Bit error rate for FSK modulation
E_b/N_o: Signal-to-noise ratio

$$\frac{E_b}{N_O} = S/N + 10 \log\left(\frac{ENB}{R}\right) \quad (94)$$

Where:
S/N: Signal-to-noise ratio expressed in dB

ENB: Effective noise bandwidth, equal to the bandwidth of the IF filter used in the FSK receiver system

R: Bit rate of $1/T_b$

Note: The S/N used in equation (94) is the signal-to-noise ratio measured at the input to the limiter stage. This is the carrier-to-noise ratio C/N calculated by equation (64).

11 References

1. Loy, Matt, *Understanding and Enhancing Sensitivity in Receivers for Wireless Applications,* Texas Instruments application note SWRA030, May 1999
2. Zeimer, R.E., Tranter, W.H., *Principles of Communications Systems, Modulation, and Noise, 4th Ed.,* John Wiley and Sons, 1995
3. Stremler, Ferrel G., *Introduction to Communication Systems 3rd Ed.,* Addison-Wesley, 1992
4. Couch, Leon W., *Digital and Analog Communication Systems 5th Ed.,* Prentice-Hall, 1997
5. Erst, Steven J., *Electronic Equations Handbook,* Tab Division of McGraw-Hill, 1989
6. Rappaport, Theodore S., *Wireless Communications Principles and Practice,* Prentice-Hall, 1996
7. Kaufman, Milton, Seidman, Arthur H., *Handbook of Electronics Calculations,* McGraw-Hill, 1979
8. Franceschino, Albert, *An IF Communication Circuit Tutorial,* Motorola application note, AN1539, 1996
9. Sofianos, Paul, *Practical Solutions for Medium Data Rate Wireless Communications,* Motorola application note, AN1691, 1999
10. Erst, Steven J., *Receiver Systems Design*, Artech House, 1984
11. Hsu, Hwei, *Schaum's Outline Theory and Problems Analog and Digital Communications*, McGraw-Hill, 1993
12. Razavi, Behzad*, RF Microelectronics*, Prentice Hall, 1998
13. Rohde, Ulrich L, Whitaker, Jerry C, Bucher, TTN, *Communications Receivers: Principles and Design, 2nd Ed.*, McGraw-Hill, 1996
14. Krauss, Herbert L., Bostian, Charles W., Raab, Frederick H., *Solid State Radio Engineering,* John Wiley and Sons, 1980
15. Hayward, Wes, *Introduction to Radio Frequency Design,* American Radio Relay League (ARRL), 1994
16. Dao, A., *Integrated LNA and Mixer Basics,* National Semiconductor application note, AN-884, 1995
17. Meador, Don A., *Laplace Circuit Analysis and Active Filters,* Prentice Hall, 1991
18. Trofimenkoff, F.N., Treleaven, David H., Bruton, L.T., *Noise Performance of RC-Active Quadratic Filter Sections,* IEEE Trans. Circuits Theory, vol. CT-20, pp. 524-532, Sept.1973
19. Sklar, Bernard, *Digital Communications Fundamentals and Applications,* Prentice-Hall, Inc. 1988
20. Johnson, Howard, Graham, Martin, *High Speed Digital Design: A Handbook of Black Magic,* Prentice Hall, Inc. 1993
21. *Analog Devices: Technical Tutorial on Digital Signal Synthesis*, Analog Devices, 1999.
22. *TRF6900A Single-Chip RF Transceiver*, Texas Instruments data sheet SLAS258, May 2001.
23. Peebles, Peyton Z. Jr., *Digital Communication Systems*, Prentice-Hall, 1987.
24. Rohde, Ulrich L., *Microwave and Wireless Synthesizers: Theory and Design*, John Wiley and Sons, 1997.

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