Computer-aided design of printed circuit board

Introduction

At the beginning of the 20th century, the components of early electrical devices were soldered to riveted solder “tabs”, and the individual components were connected by insulated wire. This manufacturing technology was extremely time consuming, could not be automated at all, and there was a high potential for error during manufacturing. These problems were recognized in the early 1900s, and manufacturers started to develop new component assembly technologies. The development of printed circuit assembly technology in the modern sense was initiated by Paul Eisler in the 1930s. From the 1960s to the present day, this type of assembly technology has become almost dominant.

A printed circuit board (PCB) is a network of solder points made of metal foil applied to the surface or surfaces of an insulating plate, connected by conductive strips. The components are soldered to the soldering points, the electrical connections are provided by the conductive strips. The sheets can be rigid or flexible, single, double or even multi-layered. In some cases, connector and switch contacts can also be made of metal foil. The components can be Surface Mounted Device (SMD) or Through Hole Device (THD) components.

There are several types of manufacturing technologies for printed circuits. The subtractive (film etching) method is the most widely used. In this method, the surfaces of the mounting plate covered with copper foil, which will form the circuit, are provided with an etch-resistant protective layer, and then the remaining copper is chemically released. The semi-additive process is also used in large plants. The plate used here contains only a very thin layer of copper. The holes for the plate are pre-drilled with a CNC drilling machine. A layer of metal is galvanized on the plate and on the chemically treated inner wall of the prefabricated holes (only where the circuit design requires it, of course). The electroplating material may be tin or a tin-lead alloy. Excess copper is then etched off. The etchant does not react with tin and lead, thus forming the designed wiring system on the surface. With this method, the walls of the holes can also be metallized, which makes it possible to make two- or multi-layer circuits. Additional layers can be created on the printed circuits above the conductive metal layer: for example, a solder mask layer to facilitate soldering of the components and to insulate the wires (Soldering Mask), and a Silk Screen layer for the data and shape of the components to be implanted.

The same main design steps are required for small-scale and large-scale processes:

- specification of the circuit, selection of components based on the specification,
- design of the circuit diagram,
- simulations,
- product design: design, size of the printed circuit board layout, location of controls, boxing, etc.
- documentation.

In the last three to four decades, computer-aided design (or CAD for short) is used to provide a faster, more efficient, and possibly error-free design. The purpose of the laboratory exercise is to present these design steps using a common circuit design program.

The purpose of the measurement is to present the OrCAD design system and the main steps of printed circuit design.

Theory and basic concepts and terminology

Components:

In OrCAD, the same software module is responsible for selecting the circuit components and designing the circuit itself: OrCAD Capture CIS (Component Information System) Lite. In OrCAD CIS, under the "Place Part" option, you can choose from thousands of circuit drawing symbols.

The components are grouped into Libraries. Each component has a number of parameters that you can edit yourself with the appropriate module in Capture CIS. Examples of such parameters are the names and enclosures of the components, the component footprint of the circuit diagram, and the parameters of the PSpice simulation.

Footprints

In order for a component to be soldered to the circuit board and wired together with the other components, a component-specific copper foil design, the so-called footprint is required. A footprint is practically a set of contact surfaces corresponding to the legs of a part, as well as the corresponding markings. Each part comes with a footprint. For example, a footprint of a surface-mounted resistor is two pieces of square copper foil of a given size (pad, contact surface) spaced apart. A footprint of a through hole resistor is two circular copper foil fragments of a given size with a metallized wall hole of a given size in the center. Figure 2-1 shows these elements. Footprints appear as separate objects in all circuit design CAD systems. Wiring is formed between the footprints.

You can draw the appropriate footprint for each component yourself, but there are also predefined footprints for the more common components in the software libraries.

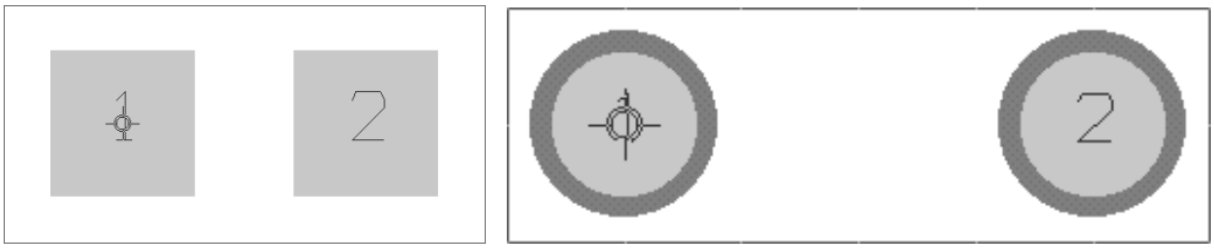


Figure 2-1: Footprints of an SMD (left) and through hole resistor (right).

Netlist

The netlist file connects the circuit diagram to the circuit wiring diagram. This file lists the component legs that specific nodes are connected to. With the help of the net list, it is also possible to port your design to another circuit design software family.

Layer

As mentioned in the preface, a printed circuit board can have several layers:

- wiring can be included on the top and bottom layer s(TOP and BOT),
- Solder Mask varnishing on both sides (SMT, SMB),
- silk screen captioning on both sides (SST, SSB),
- stencil aperture (SPT, SPB) that can be defined for surface mounted devices,
- for multilayer circuits, internal wiring layers (PWR, GND, INNER layers).

Circuit design programs usually treat the mounting plate perforation (DRD, NC Drill), the factory label (FAB) or the NOT notes as a separate layer. (If necessary, you can also define additional layers.) These layers are marked with separate colors in the wiring diagram. You can see each layer in a top view.

The above abbreviations are examples only, but are typically similar in all circuit design CAD software.

Back annotation

Back-annotation can mean back-reference and modification, but it can also facilitate mass production as one of the final steps in printed circuit design. For example, you can rename components and then trace this change back to the wiring diagram. This is because the components on the finished circuit board are often not in the same structure as in the circuit diagram, which makes it difficult to find and insert the next component in case of manual implantation.

Gerber file

Gerber files are data files that contain direct information for the computers in the production lines. These files can be used to directly control, for example, the drill, screen maker or contour cutter. There are several file formats, such as ARISTO, EUCLID, MEDUSA, ROMULUS. The GERBER file format is one of the most widely used.

Additional notions

- Via: a hole that makes metallic contact between two wiring layers.
- Pin: A pin is the end point of a wiring diagram. Usually this is a component foot, but it can even be a measuring point.
- Pad, padstack: the physical design of the pin on the surface of the circuit.

Conducting rules

- With current technologies, an average circuit manufacturer can make wiring 6-8 mils or thicker (1 mil equals 25.4 µm, one thousandth of an inch). For simpler circuits, 8 to 12 mil wires or even wider are commonly used.
- The power cords are usually sized a few times thicker than signal cords because much more current flows through them and the voltage drop across the thin cord can be too large, which can interfere with the operation of the device. During professional design, the cables can be sized according to the maximum current demand of the active components.
- Wiring is never broken at right angles, it is usually bent at a 90 + 45 degree angle. This is necessary because in the case of a sharp break, the corners are rounded due to the imperfection

of the manufacturing technology. The right angle can also cause a corner effect in the current path.

- With the exception of very densely designed panels, it is not advisable to use a hole diameter of less than 0.6 mm, because as the hole diameter decreases, the number of plates that can be drilled in one bundle decreases, which significantly increases the price per unit area.
- When specifying hole diameters, keep in mind that there are no drill bit diameters available for all kinds of numerical values, and having 10 to 12 types of holes in a single panel also increases drilling time and manufacturing costs.
- For a hole-mounted part with a given outlet diameter, do not define a hole in the panel as large as the diameter, but a larger one, because due to the hole galvanizing, the actual size of the hole will be smaller than the diameter of the drill bit used. (It is a good idea to check the manufacturer's information on hole plating.)
- On films required to make a solder resist lacquer coating, it may be worthwhile to increase the coverage of the pads (i.e., the aperture on the varnish) relative to the size of the pad on the panel. Depending on the technology and requirements used, a larger aperture (non-solder mask defined pad) can be defined, but even a smaller one can be defined also (solder mask defined pad). Technology is dependent on the latter case e.g. whether the entire pad is enlarged to retain the original surface.
- Do not drill a hole closer than 1 raster (0.1 inch, or 2.54 mm) to the edge of the panel and do not bring a wire closer than half a raster, as they may be damaged during cropping or contour milling. Of course, these rules may be influenced by mechanical and device design considerations.
- Make sure the connection of the wires to the bench is clear. Avoid T-shaped or backward-connecting wiring. If possible, use a rectangular or 45-degree wire guide at the corner of the bench.
- In the case of double-sided panels, try to make the surface of the pads and conductor strips to be nearly the same for better surface utilization.

Measurement tasks

1. Create a circuit diagram in OrCAD Capture CIS Lite

After starting the Capture CIS Lite module, you will see the Start Menu window. In addition, the LOG window also appears at the bottom of the screen, where the program displays various events to the user. Creating the circuit diagram starts by opening a new project (File-> New-> Project / or selecting the appropriate icon in the Start Menu). Use the PSpice Analog or Mixed A / D wizard.

Important: Do not use accented characters and special symbols in the program, including the name of the home folder. Note that lowercase and uppercase letters are distinguished characters.

For example, Let the name of the project be “Amplifier”. It is also important to define the working folder (Location -> Browse…), which is typically created on the student (D:\) drive. In the pop-up window that follows, make sure that the demo_all_libs.opj file is selected, which will automatically add the most important component libraries available to the project. Finally press OK.

After creating the project, new subdirectories and files are created in the folder: a project file with an .opj extension, which contains the project settings, and a design file with an .dsn extension, which will

contain the circuit diagram to be designed and its settings. A folder containing PSpice files is prepared for the simulation.

The Amplifier project window appears on the screen with a new tab. All files and information related to the project are located in a directory structure in the project window. Within Design Resources you can find the Library and amplifier.dsn. The Library contains loaded library files when you open the project. There are two additional subdirectories in the amplifier.dsn "directory", one of which is named SCHEMATIC1, which contains the circuit diagram. Rename SCHEMATIC1 to AMPLIFIER (right-click) and change the PAGE1 entry in the AMPLIFIER directory to AmplifierA. In the Schematic Page Properties menu, right-click AmplifierA, set the size to millimeters on the Page Size page, and then select A4 paper size.

The Design Cache is on the same level as AMPLIFIER. This library will contain information about the parts used in the design. Double-clicking on AmplifierA will bring up the circuit diagram. Here you can design the inverting amplifier circuit shown in Figure 2-2.

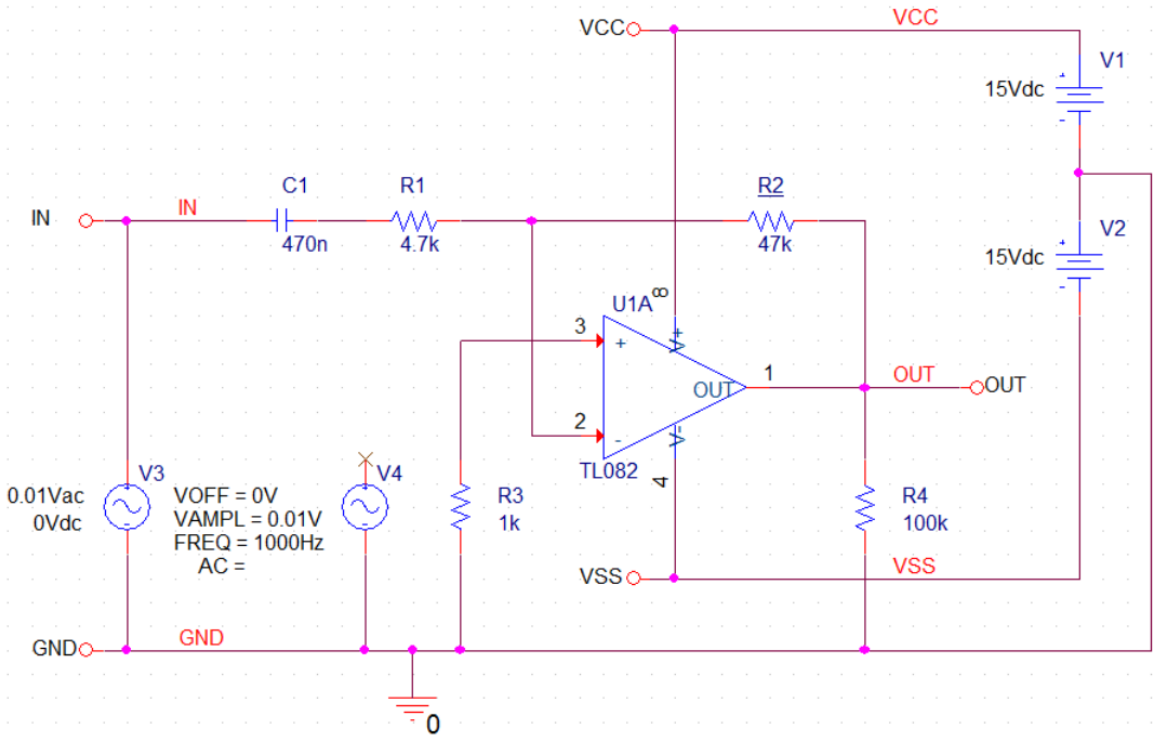


Figure 2-2 Wiring diagram of the inverting amplifier

The task begins using the "Place Part" menu item on the right toolbar. The menu can be accessed by pressing the P button or via the icon on the right side of the screen (. Parts have be collected from multiple files. For example, you can search for a resistor in the Place Part window that pops up on the right with the Part Search command. In the Libraries window, select the ANALOG folder (if it is not visible in the Libraries list, you must add the analog.olb file in the Pspice Windows subfolder with the button), and then type R. You can drop the R part that appears by clicking the icon (above the Part search box. (This icon looks the same as the icon on the far right toolbar.)

The cursor has changed and it can be seen that a resistor can be placed with it. Rotate the resistor if necessary (R key) and place it. The cursor is still moving with the resistor. Place the other resistors according to the wiring diagram and exit with Esc. The next task is to find the operational amplifier. You can find the TL082 part in the OPAMP folder. For parts with more specific names, selecting all directories can speed up the search process.

You can also add library folders downloaded from the Internet (provided by the manufacturer) to the plan using the buttons in the Libraries section.

Finally, look for capacitors (C) in the ANALOG folder as well. You can change the value of the placed parts by clicking on them. Enter the appropriate parameters according to Figure 2-2. Note that the program is able to interpret the 100k syntax too. Use the dot character as the decimal point if needed.

By clicking once on the parameters that can be seen on the screen their position can be adjusted, and their value can be modified after double-clicking. If necessary, the Property Editor window can also be reached by double-clicking on a part symbol. (See later.) From this point, save your project frequently.

The PSpice simulation will later require a supply voltage and two special signal sources. These have to be placed like the resistors. The supply voltage is VDC, while the two special sources are VSIN and VAC in the SOURCE directory. Set 15Vdc for VDC generators. For the VAC generator, set 0.01V AC voltage and 0V DC voltage, for the VSIN generator, set 0V offset voltage, 0.01V amplitude and 1000Hz (do not hit space between the numbers and the unit). Connect the VAC generator to the input. Connect the VSIN generator to the lower node, but do not connect it to the input. Instead, place a Not Connected mark on its other node ( icon on the rightmost toolbar).

Connections between parts can be made using Place-> Wire (W, or toolbar icon  . Two wires are only electrically connected to each other if the connection is indicated by two small pink dots at the ends of the selected active wire piece.

Additional connection points can be created in Place-> Junction (J or ). Do not forget to make the nodes shared at the output and the cable above R4! (See Figure 2.2!) The ground signal must also be placed during wiring. This can be done with the Place-> Ground (G) menu item or the corresponding toolbar icon ().

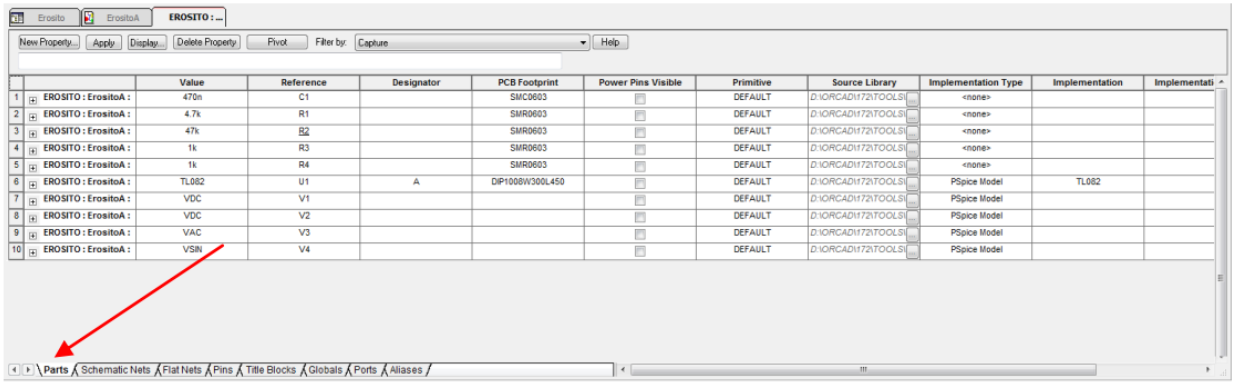
In the Place Ground window, click Add Library to add the capsym.olb file in the Library folder (this is the default) to the system, and then select the ground named (0) from this folder. Then add port markings to the figure to help interpretation. (VCC, VSS, IN, GND pins). These can be done from the CAPSYM folder of the Place Ground menu item that appears when you press the ground icon, each item will be obtained from the renaming of VCC / CAPSYM. Let's keep working: so we can name the pins by placing, rotating and renaming the VCC element. This will define a name for the associated nodes.

For faster use of the software, it is worth noting that group assignments can also be performed on parts. Select the parts by holding down the left mouse button. After pressing the right mouse button, selecting Edit Properties ... will display the Property Editor window.

Because the wires are also selected, you may see Schematic Nets may be visible by default on the bottom labels (these are tabs such as the tabs that select the bottom worksheet in Excel). Click the Parts

tab, as shown in Figure 2-3. With the "Filter by: Capture" option (or by default in the <current properties> option) all parameters of the components can be viewed and edited. Use the Pivot button to interchange rows and columns. If the parts are not visible under Parts, close the entire chart on the main tab above. Re-select the entire plan and open the Property Editor again.

Encapsulation assignment information for the parameters of the components in Property Editor is stored in the PCB Footprint field. Set smr0603 for resistors and smc0603 for capacitors. For the operational amplifier, use the DIP1008W300L450 footprint. (The names of the footprints can be understood from the abbreviations: SM - Surface Mount, DIP - DIP housing, etc.).



		Value	Reference	Designator	PCB Footprint	Power Pins Visible	Primitive	Source Library	Implementation Type	Implementation	Implementati
1	EROSITO : ErositoA :	470n	C1		SMC0603		DEFAULT	D:\ORCAD\172\TOOLS\	<none>		
2	EROSITO : ErositoA :	4.7k	R1		SMR0603		DEFAULT	D:\ORCAD\172\TOOLS\	<none>		
3	EROSITO : ErositoA :	47k	R2		SMR0603		DEFAULT	D:\ORCAD\172\TOOLS\	<none>		
4	EROSITO : ErositoA :	1k	R3		SMR0603		DEFAULT	D:\ORCAD\172\TOOLS\	<none>		
5	EROSITO : ErositoA :	1k	R4		SMR0603		DEFAULT	D:\ORCAD\172\TOOLS\	<none>		
6	EROSITO : ErositoA :	TL082	U1	A	DIP1008W300L450		DEFAULT	D:\ORCAD\172\TOOLS\	PSpice Model	TL082	
7	EROSITO : ErositoA :	VDC	V1				DEFAULT	D:\ORCAD\172\TOOLS\	PSpice Model		
8	EROSITO : ErositoA :	VDC	V2				DEFAULT	D:\ORCAD\172\TOOLS\	PSpice Model		
9	EROSITO : ErositoA :	VAC	V3				DEFAULT	D:\ORCAD\172\TOOLS\	PSpice Model		
10	EROSITO : ErositoA :	VSIN	V4				DEFAULT	D:\ORCAD\172\TOOLS\	PSpice Model		

Figure 2-3. The Property Editor window.

At this point, it is important to note that the type of the required footprint can be looked up: Orcad 17.2 stores factory footprint files in the following folder (The location of the resulting directory may differ depending on the installation location):

\Cadence\SBP_17.2\share\pcb\pcb_lib\symbols

Getting the footprints this way is not practical, especially since the user does not see the dimensions of the relevant footprint. Moreover, it may be necessary to overwrite the factory footprint and create a new one. This will be possible later in the PCB Editor Lite, where by selecting the New / Package Symbol Wizard option, the program will help the user to create a new footprint with a wizard. You can check the size of each footprint in PCB Editor Lite. We will not go into the details during the laboratory.

For ordered parts, the manufacturer generally offers footprint files for use in Orcad / Allegro, and often 3D Step models too. Footprint files downloaded from the manufacturer must be placed in the folder mentioned above.

For the subsequent node references, use the Place-> Net alias (N,) menu item to place VCC, VSS, IN, and OUT labels on the appropriate wires. The program performs the assignment by assigning the label to the wire closest to it (the frame of the label must be in contact with the wire!), To avoid misinterpretations, do not place a label near wire crossings.

The usefulness of Net tags is demonstrated by the fact that the density of complex cross-wiring can be made more transparent by using logically placed tags. This requires naming the free-hanging wires with a common label. Figure 2-4 shows the circuit of Figure 2-2 using Net labels. It is not necessary to redraw our plan for the solution shown in Figure 2-4, we only wanted to show an alternative option.

By placing the appropriate labels, the schematic diagram is ready to perform the simulations. Attention, it is not possible to perform simulation on all circuit designs, only those circuits can be simulated where the corresponding PSpice models are available. These are often provided by component manufacturers on their websites. In the present example, we are looking at an analog circuit, so it is reasonable to perform an extensive analysis on the circuit.

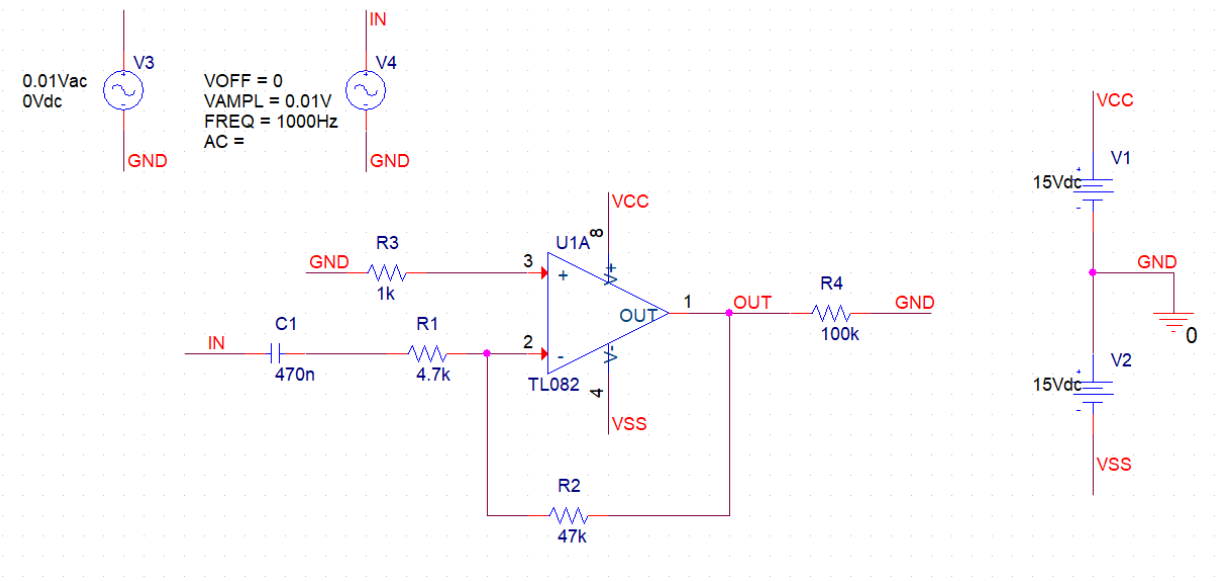


Figure 2-4. Alternative wiring using labels.

2. PSpice simulation

In Capture CIS Lite, click the PSpice menu and select Create Netlist. As a result of the instruction, if you did everything right, the program will generate a file with a .net extension, which can be viewed in the Outputs directory in the project window.

For each simulation, a simulation profile must be created in the PSpice menu with the New Simulation Profile menu item. You must enter a name for the new profile, which should be "OperatingPoint", and then confirm it with the Create button. When the profile is created, a window will appear with the settings related to the profile. Here you can specify which simulation you want to perform (Operating point, transient, etc.).

On the Analysis tab, the Analysis type must be set to Bias Point, the default settings are fine for the other parameters. Press OK to save the created simulation profile.

The simulation profile is located in the PSpice Resources / Simulation Profile directory in the tree structure of the project window. By right-clicking on the name, you can change the profile settings (Edit Simulation Settings) and even run the given profile from here.

Before running the profile, right-click on the new profile in the project window, select Make Active from the pop-up menu to confirm the active status of the selection.

By default, the newly defined simulation profile is activated, but the user may click aside, so always make sure the right profile is activated!

The simulation can be started with Pspice-> Run (or F11). If we did everything right, the status text window (bottom line) of the pop-up PSpice A/D program will display that it ran without error. (Bias point calculated.)

You can view the result in Pspice A/D by selecting View-> Output File. The window contains a complete description of the circuit with PSpice notations and all the operating point data at the bottom of the page (Figure 2-5). Notice that the individual node voltages also appeared in the schematic diagram of Capture CIS! (See Figure 2-8 later.)

```
 ** Profile: "EROSITO-Munkapont"  [ C:\BME\Labor\Erosito_jegyzethez\Erosito-PSpiceFiles\EROSITO\Munkapont.sim ].

 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

*******************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(   IN)    0.0000  (  OUT)-24.02E-06  (  VCC)   15.0000  (  VSS)  -15.0000
(N00285)-13.92E-06 (N00289)-13.92E-06 (N00451) 215.0E-09 (X_U1A.6) 2.263E-09
(X_U1A.7)-24.04E-06                   (X_U1A.8)-24.04E-06
(X_U1A.9)    0.0000                   (M_UN0001)    0.0000
(X_U1A.10)     .3992                  (X_U1A.11)   14.5750
(X_U1A.12)   14.5750                  (X_U1A.53)   12.6840
(X_U1A.54)  -12.6840                  (X_U1A.90)-455.2E-09
(X_U1A.91)   40.0000                  (X_U1A.92)  -40.0000
(X_U1A.99)    0.0000


    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_V1        -2.283E-02
    V_V2        -2.283E-02
    V_V3         0.000E+00
    V_V4         0.000E+00
    X_U1A.vb     2.263E-14
    X_U1A.vc     1.269E-11
    X_U1A.ve     1.442E-11
    X_U1A.vlim  -4.552E-10
    X_U1A.vlp   -4.000E-11
    X_U1A.vln   -4.000E-11
    TOTAL POWER DISSIPATION   6.85E-01  WATTS


          JOB CONCLUDED
```

Figure 2-5. Operating point data of the designed circuit

Determine the consumption of the circuit. Which component dissipates the most power?

To perform frequency domain analysis, create a profile called AC. Its type should be AC Sweep / Noise (you can create a Bode diagram representation using that). The frequency shall be logarithmically plotted from 1 Hz to 10 MHz (enter 1 and 10 meg), with 5 plots per decade. Run the profile. After that, the output voltage must be displayed: in Pspice AD, a new output diagram can be added using the Trace-> Add Trace menu item (Figure 2-6). To plot the amplitude of the Bode plot, select DB () in the Functions and Macros column of the window that appears, then V(OUT) in the Simulation Output Variables column and divide it by V(IN). (Parameters are easier to find when the Currents and Alias Names boxes are turned off.)

Alternatively, you can plot the figure by typing DB(V(OUT)/V(IN)) to Trace Expression. You can copy the image using Window-> Copy to Clipboard.

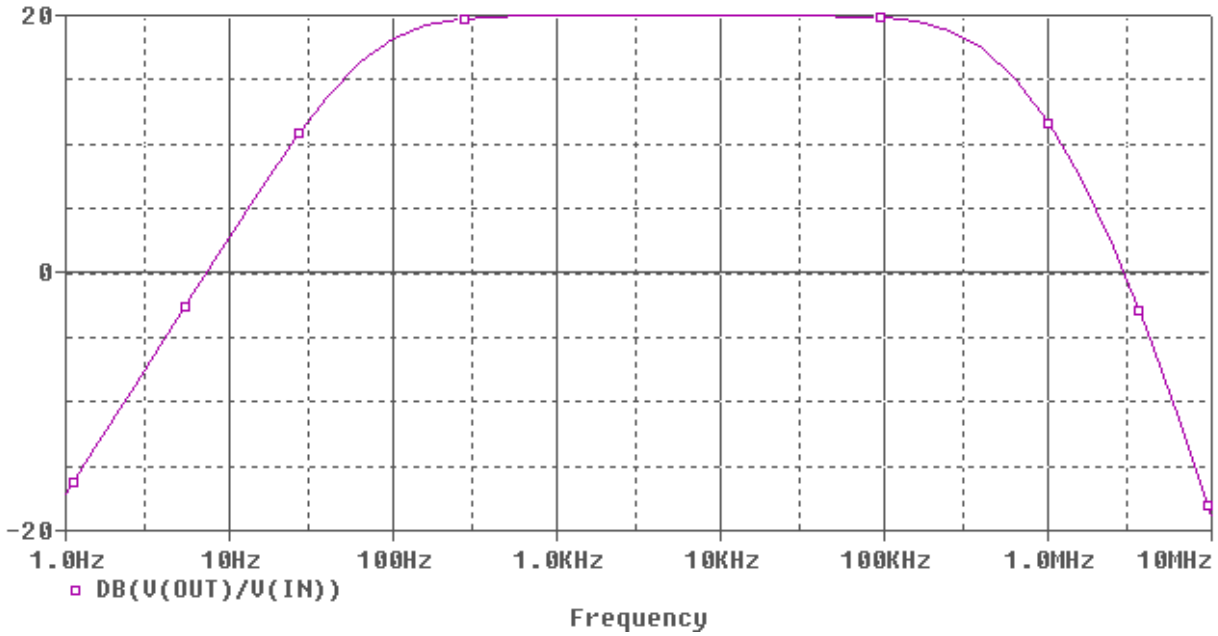


Figure 2-6. Amplitude characteristics of the designed circuit

Study the result. If you have time, plot the phase response of the circuit.

To create the third, time domain analysis profile, you need to modify the circuit diagram in OrCAD CIS: connect the VSIN generator, and close the VAC generator with the NC (not connected) option. Create a new profile called "Transient". Set the Analysis type to Time Domain (Transient) and set “Run to time” to 5 ms. Remember to verify the active status of the Transient profile.

Run the simulation and in Pspice AD, add the V(IN) and V(OUT) signals to the Plot figure in the Trace-> Add Trace menu. Study the result (Figure 2-7).

The figure can also be created by starting the simulation in the Capture CIS window by placing the voltage measuring probe of the toolbox on the wires of the IN and OUT nodes. (Top toolbar,  icon.) Did you get the output curve you expected?

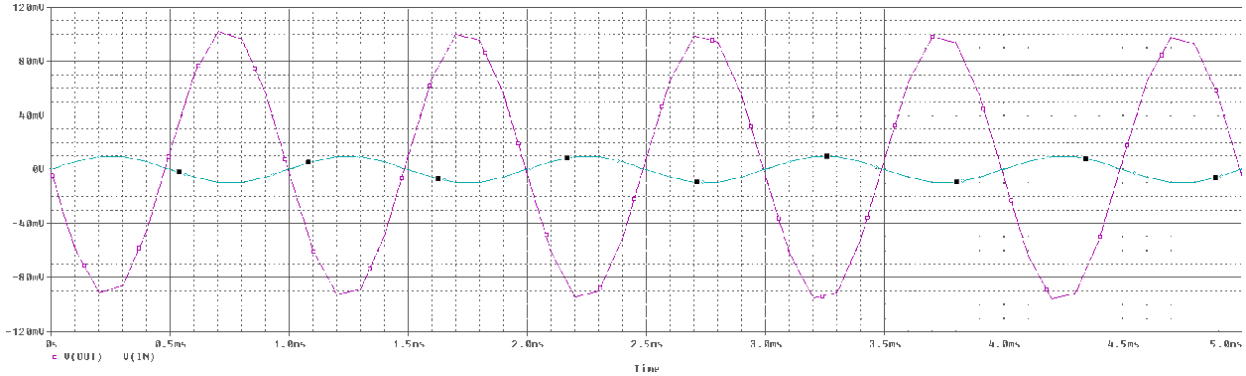


Figure 2-7. Transient analysis of the circuit.

3. PCB editor

In addition to the simulation, the actual physical design of the circuit must also be prepared.

Items that only appear in PSpice do not need to be deleted. (E.g. the sources.) In reality, the sources must be connected somehow to our circuit, e.g. the +/- connectors of a battery or a header to which a power supply can be connected. The connection to the panel can also be realized with test points, but if you want to solder by hand or work with a measuring probe, touching the test point plane is not practical at all.

It may be better to design a standard connector or a row connector. We will fit a standard (100 mil) connector to our plan. The connector can be used with a sleeve cable or with measuring clips.

To do this, add the appropriate component to your plan with the library name HEADER 5 from the CONNECTOR directory (if not added, add it to the plan: it can be found in a folder one level higher than the PSpice folder!). Enter "BLKCON100VHTM1SQSW1005" for the connector footprint. Assign the VCC, VSS, GND, OUT and IN wires to the connector pins. Figure 2-8 shows the modified schematic diagram. Save the changes.

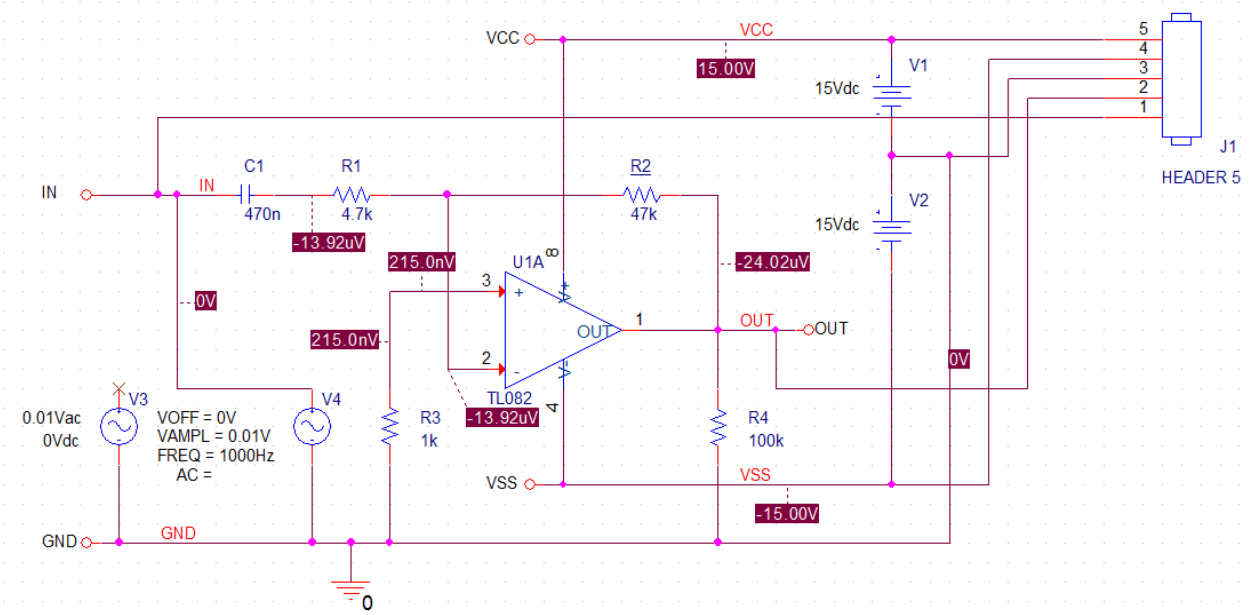


Figure 2-8. Adding the connector to the design.

In the main hierarchical project window, make the amplifier.dsn file active (that is, select it), and then click the PCB tab in the window that appears in the Tools-> Create Netlist menu. Here we create the netlist file, which on the one hand provides a gateway between the two softwares and on the other hand includes the components and nodes of the circuit plan. Make sure the Create PCB Editor Netlist option is checked in the default settings. Then create a Netlist Files Directory: let the folder name be Amplifier_PCB.

Press OK to generate the netlist. In the folder defined for PCB designs, three files with a .dat extension appear among the output files; they contain all the necessary information about the circuit designed in

Capture. It is recommended to close the PSpice program at this point so that the many open windows will not confuse you later.

After starting the OrCAD PCB Editor, open a new window with File-> New. The program asks the first questions about the plan. The type shows that you can create a board, a module, or even a footprint (Package symbol). The (wizard) mark means that you can navigate through the basic tasks in a Windows Wizard-type menu bar.

Select the Board (wizard) option and name it Amplifier_PCB and select the appropriate folder. Press OK. Click Next in the first window. With the help of the Board Template you can load a pre-made panel template. We don't need this, so press "No" and (Next>). We do not want to assign an optional tech or optional parameter file to our plan (Next>). The optional board symbol (mechanical drawing) that pops up in the next point is also omitted now (Next>). The design unit should be Mils, the size of the drawing sheet should be A, and the origin should be in the lower left corner. (Next>) The accuracy of the grid spacing in the background can be 25 mils, and we will need two etched (etch, i.e. copper on the surface of the substrate) layers, for which “default” films should be generated by the program (Next>). The Top and Bottom layers will be OK by default (Next>), and in the following we can specify the minimum wire width, the distance between the wires (line to line), the distance between the wires and the pads, and the distance between pads. Configure 8 mils on each. For Default via padstack, select single (via) from the … list, press OK, then (Next>). In the following, you can set the panel to be rectangular (Next>), and then specify a width (W) and height (H) of 1000 mils. No corner cutoff is required, but it may be worthwhile to set the 50 mil distance between wire and panel edge (Route keepin distance). Set a distance of 100 mil between the component and the panel edge (Package keepin distance), press (Next>), then Finish.

The panel will appear on the new surface, where the actual edge will be dark green, the keepin marking will be light brown, and the component marking will be purple by default. You can check the colors in Setup / Colors (CTRL + F5). (The outer frame of the disc is colored by Geometry / Board Geometry / Design Outline, and the wiring and component placement can be repainted at Areas / Route and Package Keepin.) If you don't see the panel, check the View map.

The handling of the interface is very similar to the functions seen previously in CIS. It is recommended to use the zoom functions on the top toolbar and the mouse wheel. You can move over the plan by pressing the mouse wheel and moving the mouse.

Now import the netlist. In the menu bar above, select Import / Netlist and then the Cadence tab to set the following: Design entry CIS, Import directory (select Amplifier_PCB), then Import Cadence. The log will notify you if the import was successful. Close the log and Import windows.

Figure 2-9. shows that six different functions can be selected on the toolbar. These are from left to right: General, Placement, Etch, Signal Integrity, RF editing (this cannot be selected with the current settings), and Shape editing. By selecting these, the program will automatically sensitize our cursor to edit the specified items.

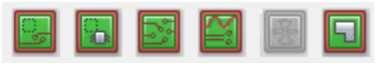


Figure 2-9. Toolbar options.

Select the Placement edit option, then select Place / Quickplace from the menu bar above. In the pop-up window, press the Place button: as a result, all the components will be placed on the desktop. Close the Quickplace window with the Close button. (The upper right X of the window removes the parts.) In the selected Placement edit mode, the parts can be positioned on the given grid as well as rotated (right click, rotate).

You can refine and roughen the grid (the raster on which the cursor moves) in Setup / Grids. The grid can also be made visible here (Grids On).

During design, sometimes designers notice problems at a later stage. In the current plan, depending on the load, the presence of R4 resistor might be a problem. To remove it, return to the Capture CIS interface and delete the R4 part. Remove the remaining wirings, and then generate a new netlist. In the PCB Editor, perform the import operation again, leaving all options with the previous settings so that the plan is updated according to the modified netlist. With this method, footprint replacement and part replacement can also be performed.

Alternative way: There is another way to keep the R4 resistor, as it may be necessary for later simulations. In Capture CIS, double-click the load resistor, then in appearing the window click the New Property button in the button bar above. Then enter a name for the new property: PSpiceOnly. Set the value of the new column to TRUE (case sensitive). Generate a new netlist for the layout, then return to PCB Editor and import again. Now the load resistor does not appear on the screen. If you want to add a new part on your desktop, don’t forget place it in Quickplace or manual placement mode.

Try placing the SMD components on the Bottom side and placing one under the DIP case. This is not a problem, as the encapsulated part of the through hole part will be at the Top layer, and the solder side at the Bottom. You can switch layers using right-click - Mirror.

You may want to add a part with the cursor when the drawing of the part under the cursor changes its color. The current operation can be turned off with F9 or right click and Cancel option.

Figure 2-10 shows an example of the finished panel for placement and wiring. Note that the two layers (Top / Bot) are marked with different colors and that the labels on the bottom (and, if applicable, the part footprints) are mirrored.

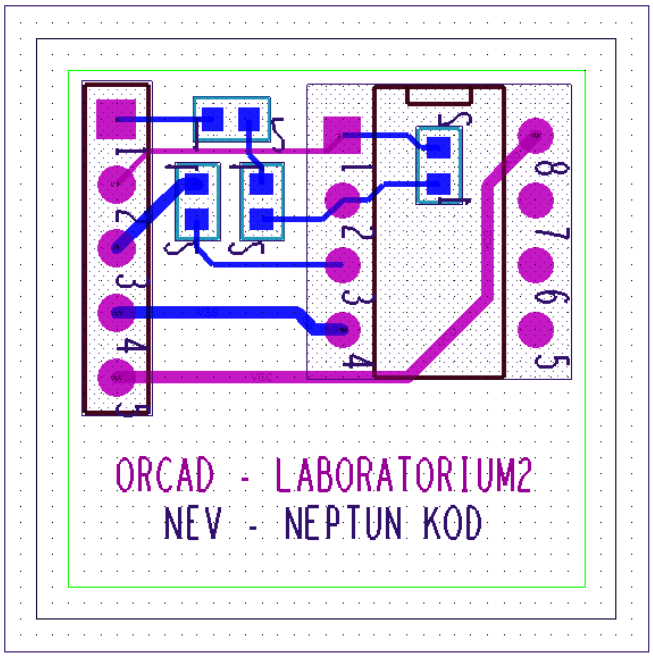


Figure 2-10. Finished PCB design - with placement, wiring and label suggestions (colors inverted).

However, before you start wiring, you may want to define the width values for the wires more precisely in the Setup / Constraints menu. With the above option, start the Allegro Constraint Manager window, where you can define the various rules of your plan in detail. Look for the Physical button in the Worksheet Selector window on the left (If Electrical is open, Physical may be in the lower direction of the screen with the Spacing, Same Net…, etc. buttons by default).

Expand the Physical option, select the Physical Constraint Set / All Layers option by double-clicking, look for the DEFAULT setting. Right-click on DEFAULT, Create (PhysicalCSet) and create a constraint set called POWER, where you set the Line Width minimum to 20. Then look at the Net / All Layers option on the left. For nodes VCC, VSS, 0 (i.e., ground), set POWER in the Reference Physical CSet column. The power cords will then be forced to a width of 20 mils.

If there are many nodes, you can also group them by selection. Create a Group by selecting the VCC, VSS, 0 nodes, then right click, Create / Net Group. Here enter POWER_TYPE as the Net Group name. Hierarchical ordering is then clearly seen for the supply type lines.

Return to PCB Editor, the next step is wiring. We start by selecting Etch edit (referring to Figure 2-8) so that we can easily indent the common nodes waiting to be connected to the Rats. To do this, look for the Add Connect option on the left toolbar ( )

When you drag the wire, you can observe that the program thickens the Power-type lines by default, interactively bypasses obstacles, and can even push other wires away to fit the new wiring. This option can be changed during wiring in the option window on the right. (This option window will be monitored frequently from now on.) While wiring with the Bubble / Shove function, you can shift an already connected wire under the given distance rules; and the Hug option is for smoothing wires next to each other under specified rules. By disabling these options, you can arbitrarily arrange the wiring (this might introduce errors in the design). The Hug / Shove option works best when we are on a 1 mil grid. This

might cause the visual grid becoming very dense - in this case, you may want to turn it off (Setup / Grids / Grids on). For fully manual wiring (Hug / Shove is off), it is a good idea to manually select the resolution of the wiring grid while working.

The option window otherwise contains many useful features during active wire drawing. The Line lock feature can be interesting now, which fixes the breaking angle of the drawn lines in 45 degrees, or the width adjustment, where the width of the given wires can be scaled manually.

If you do not have an actively drawn wire, but you are in Etch edit mode, (in this case Etch will be the active class in the Option menu on the right), you can switch between the Top and Bottom pages, making it easier to select the starting wiring side.

You can also switch layers by right-clicking while drawing a wire. (This is only allowed by the software if you want to do a logically correct thing: when connecting a SMD part placed on the bottom side, you can't suddenly switch to the Top layer without via, while when installing a hole, you can use both copper layers for the connection.) With a right click we can also put a via during wiring (or by double clicking) if needed.

If you have not been able to place or modify a piece of wire correctly, you can gently move the line further by pressing the mouse button. The easiest way to delete a wire is to select the wires to be deleted by default by selecting a polygon (that is, drawing a rectangle while holding down the mouse button), then right-clicking and Delete. (Alternatively, you can type delete in the command line below.) You can change the selection options in the right-click / Selection Set option on the blank worksheet.

At this point, you can see that even on this small circuit board, there is plenty of free space left, so it's worth unpacking some captions with the toolbox text tool () on the left. These can be resized in the Setup / Design Parameters Text tab. Here Orcad handles different types of captions in a block-like manner. For the name, neptun code, etc. captions the default first block is used. Modify the scaling to W: 25.00 / H: 40.00In the Setup text sizes menu. The Photo Width should be 6.00 mil wide.

When placing captions, be aware that the text is placed on the copper layer by default. To switch to the screen layer, select Active Class and Subclass / Component Value in the options window on the right side of the text input tool and Silkscreen_Top in the drop-down window below. Try to put the bottom caption this way. Select a part on the first click, which will have the caption according to the database, then define the location of the caption on the second click, and then you can write the text. (Name, Neptun code, …) If all goes well, the color of the text will be the same as the color marked for the screen layer in the options window. As a final step, you may switch to General Edit mode, right-click / select Text within the Super Filter option, and use the text-sensitive cursor to select unnecessary blue encapsulation numbers (Ref Des data - these are not needed now), then right-click / delete. Pin numbers can be moved to the appropriate location with a little positioning. The main consideration is that there should be no number above the pin (but it can be above a wire).

4. Production files

As a final design step, we need to create the Gerber files needed for production (drill file, Top / Bottom layer pattern, etc.).

Before generating the production files, use Check / DRC Update to make sure that you are not violating your own set of rules somewhere. (This would be indicated in real time by small red markers on the

desktop.) Then, if there is no error, the production files are generated after clicking on the Export / Gerber tab. This window is the so-called Artwork Control Form. On the General Parameters tab, the Gerber RS274X format should be checked, and on the Film Control, the BOTTOM and TOP pages should also be checked.

We also want to add the edge geometry to the design. You can do this by right-clicking on any of the film layers present and then selecting the Add Manual option. The name of the new film should be BOARD_OUTLINE -> OK, then select DESIGN_OUTLINE from the BOARD GEOMETRY class in the popup window.

In the next step use the previous method to add a new SILK_TOP layer to the row, adding the PACKAGE GEOMETRY / SILKSCREEN_TOP layer, the PACKAGE GEOMETRY / PIN_NUMBER layer, and the COMPONENT VALUE / SILKSCREEN_TOP layer to the package. The SILK_BOT layer is created in the same way.

Create SOLDERMASK_TOP and BOTTOM layers in the same way as above, where PACKAGE GEOMETRY / SOLDERMASK_TOP and BOTTOM layers need to be added. In order to generate files without error, set Undefined Line Width to 6.00 in the Film Options on the right side of the Artwork Control Form. This must be done for each layer so that any line widths left undefined are managed now. Use Apertures… -> Edit-> Auto (Without Rotation) to create the D-codes that represent the geometric form of the different shapes. Close the aperture editor windows (OK, OK).

Press the large Create Artwork button. If all goes well, the generation of the files finishes successfully. Close the Artwork Control form window (OK).

The final step is the drill file. Returning to the main window, you can use the Export / NC Drill function to drill the holes. Here, enter the parameter menu with the NC Parameters key. Click Leading zero supression and Enhanced Excellon format for increased compatibility, then close the window. In the Root file name field, select your home directory, then Drill -> the drill file is created. Close the NC Drill window (Close).

The Place_txt.txt file is created for the implanter with the Export / Pick / Place Data option. Export, then Close.

Finally, the .drl and .art files must be forwarded to the circuit board manufacturer. As a verification, you may want to check the resulting files in a free online gerber viewer.

Qestions

1. What is a printed circuit board?
2. What are the main design steps in PCB manufacturing?
3. List 5 layer types.
4. From what view are circuit design programs (like OrCAD) representing the layers?
5. What is a Gerber file?
6. What is a netlist?
7. List 3 printed circuit board design rules.