PERSONAL DATA:

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LAST POSITION

2006 – Research Assistant, Budapest University of Technology and Economics, Department of Measurement and Information Systems, Budapest, Hungary
2010 – Head of Central Laboratory, Budapest University of Technology and Economics

EDUCATION

2004 – 2006 Budapest University of Technology and Economics
Department of Measurement and Information Systems
Ph.D. studies
Research project: *Hardware Architectures for Image Synthesis and Image Processing*

1996 – 2003 Budapest University of Technology and Economics (**BUTE**)
Faculty of Electrical Engineering
Major in: ***Embedded systems and electroacoustics***
Title of Ms.C. thesis: *3D Rendering Architecture in FPGA*

SKILLS

HDL Languages	*Verilog, VHDL*
	Handel-C
Programming Languages	*Assembly, Pascal, C, C++*
	HTML, PHP, SQL
CAD Tools	*Xilinx ISE, EDK, ChipScope, System Generator*
	Synplicity Synplify, Premier, Synplify DSP, Amplify
	ISSP
	Mentor ModelSim, Precision Synthesis
	Celoxica DK Design Suite
Software Tools	*VisualStudio (MFC, Win32, DirectX)*
	Matlab
Technologies	*x86, PowerPC, MicroBlaze*
	Analog Devices

PROFESSIONAL EXPERIENCE

Ph.D. research, 2004 –
Hardware Architectures for Image Synthesis and Image Processing

- Image processing architectures targeting FPGAs
- Tile based 3D rendering architecture targeting FPGAs and Structured ASICs
  - Bounding Box Bucket Sorting
  - Exact Bucket Sorting modules
    - Programmable tile size (between frames)
    - Output format allows burst reads in the subsequent modules
    - 1 tile/clock and 0.33 triangle/clock maximum throughput
  - Scalable depth/stencil buffering architecture using on-chip buffers
    - Programmable tile size
    - Based on similar Processing Elements
    - Multi pass sorting of translucent objects
    - 1 pixel/clock/PE peak fill rate for opaque objects
    - 0.5 pixel/clock/PE peak fill rate for translucent objects
  - Multisample anti aliasing using arbitrary number of samples and arbitrary sample positions

Part time projects, internships, contract works:

EVOCHEM7 (Hungary, National Research Project), 2008 – 2010
Virtual Screening

- Acceleration of the chemical similarity analysis using FPGA based accelerators (SGI RC100 and PCIe boards) and GPUs

Genome sequence assembly

- Acceleration parts of the short-read alignment process with FPGA and/or GPU based solutions

LightWare Kft. (Hungary), June 2008 –
DVI video test signal generator

- Single link DVI port output, standard and custom resolution & refresh rate support
- Progressive and interlaced output, still pictures and animation playback
- Genlock (synchronization to external video source) function
- VHDL implementation targeting Virtex-4 FX12

ProPatria Kft. (Hungary), June 2007 – February 2008
Counseling and IP development

- Hardware architecture design for glue logic/management FPGA (PicoBlaze based)
- Analog Devices Link Port interface IP with 240 MB/S/line
- Cypress USB interface IP
- General VHDL implementation, targeted for Spartan-3

Xilinx Inc. (USA), March 2006 – March 2007
2D rank filter IP core (XAPP953)

- High performance, device independent rank filter architecture
- Parametrizable VHDL implementation
  - Filter window size
  - Data resolution (per-pixel & filter value), optional filter value generation
  - Number of new samples/clock cycle (balancing complexity and operating frequency)

2D DVE IP core (cancelled)

- High performance affine transformation core with low resource requirements
- Device independent, parameterizable VHDL implementation
- Pre-scaler
  - Box filter capable of downscaling with integer ratios
  - Interface for Video Frame Buffer Controller, tuned for burst accesses
- Bilinear filter
  - Options to use 1, 2 or 4 multipliers
  - Video Frame Buffer Controller interface

Heim Systems GmbH (Germany), from January 2005
DATaRec 4 Modular Data Recording System
DIC6, DIC24 and SGU9 analog modules (6, 24 and 9channels)

- 4 cascaded FIR filter for every channel with up to 1024x decimation
- Updateable coefficients
- AC/DC compensation
- PLB Interface to an on-chip PowerPC processor
- Gigabit interface to other modules (through MGT)
- VHDL implementation targeting Virtex-2 Pro FPGA

OUT6 6-channel playback module

- 4 cascaded FIR filters with up to 1024x interpolation
- Updateable coefficients, PLB interface
- VHDL implementation targeting Virtex-2 Pro FPGA

ANH102 high speed analog record/playback module

- Single channel with 300 MHz sampling frequency
- Concurrent record and playback with up to 512 decimation and interpolation
- VHDL implementation targeting Virtex-5 FPGA

VCP100 4-channel MPEG-2 decoder module

- Employs dedicated MPEG-2 decoder chips
- Controller FPGA
  - Handles packet parsing, temporary data storage and Link Module communication

    - Custom 64-bit 16-channel programmable DMA engine for fast automatic data transfer through the PLB bus
    - Implemented in Virtex-2 Pro FPGA
- I/O FPGA
    - Vide data received from the Controller FPGA (IRIG Chapter 10 video packets) or the serial transport stream inputs
    - Transport streams are handled in HW, synchronization is done by the PowerPC CPU
    - Implemented in Virtex-4 FX FPGA

Link Module

- Main module: data acquisition and playback modules are connected to it via several Gigabit interfaces
- Accurate synchronization to external timing information (e.g. GPS, IRIG, PPS)
- Generation of timing information in various formats (GPS, IRIG, PPS)
- Clock generation for the acquisition modules
- Recording of measured data and timing information
- VHDL implementation targeting Virtex-2 Pro FPGA

Chemistry Logic Kft. (Hungary), August 2005 – November 2005
Molecule fingerprint analysis

- FPGA accelerated searching of molecule pairs in large databases, using the Tanimoto criteria
- Highly parallel, high speed implementation using Verilog HDL, Virtex-2 FPGA

EuroTech S.p.a., EuroTech Finland Oy (Italy, Finland), November 2004 – December 2006
Development of PC/104 digital I/O and communication boards

- FPGA based PC/104 peripheral boards with ISA connection
- Custom jumper-less configuration
- Verilog HDL implementation targeting Spartan-2 FPGA

EAC Gaming Kft. (Hungary)**,** January 2004 – July 2004
Display subsystem for arcade gaming systems

- Architecture definition based on specifications
- Verilog HDL implementation targeting Spartan-2 FPGAs
    - Interface to EZ80 microcontroller
    - SMC, SRAM, SDRAM controller
    - Tile based 2D display system with custom overlay capabilities and hardware animation

Publications

Péter Szántó, András Széll, Béla Fehér: *Accelerating SOLiD short read assembly with GPU*
Many-Core and Reconfigurable Supercomputing Conference (MRSC ’10)
22-24. March 2010, Rome, Italy

Péter Szántó, Béla Fehér, Attila Bérces: *Accelerating Virtual Screening of Compound Libraries*
Many-Core and Reconfigurable Supercomputing Conference (MRSC ’09)
25-26. March 2009., Berlin, Germany

Péter Szántó, Gábor Szedő, Béla Fehér: *High Performance Timing-Driven Rank Filter*
VLSI Design Journal 2008

Péter Szántó, Gábor Szedő, Béla Fehér: *High Performance Timing-Driven Rank Filter*
13. IEEE International Conference on Electronics, Circuits and Systems
10-13. December 2006., Nice, France

Péter Szántó, Gábor Szedő, Béla Fehér: *Implementing 2D Median Filter in FPGA*
VSB-Technical University of Ostrava, Mechanical Series

Péter Szántó, Gábor Szedő, Béla Fehér: *Implementing 2D Median Filter in FPGA*
7. International Carpathian Control Conference (ICCC 2006)
29-31. May 2006., Ostrava, Czech Republic

Péter Szántó, Béla Fehér: *Scalable Rasterizer Unit*
Third Hungarian Computer Graphics and Geometry Conference
17-18. November 2005., Budapest, Hungary

Péter Szántó, Béla Fehér: *Exact Bucket Sorting for Segmented Screen Rendering*
GSPx 2005
24-27. October 2005., Santa Clara, California, USA

Péter Szántó, Béla Fehér, János Lazányi: *Efficient Multi-Channel FIR Filters in FPGA*
International Carpathian Control Conference 2005
24-27. May 2005., Miskolc-Lillafüred, Hungary

Péter Szántó: *Efficient and Scalable 3D Rendering Architecture*
DATE 2005 EDAA PhD Forum
7-11. March 2005., München, Germany

Péter Szántó, Béla Fehér: *High Performance Visibility Testing with Screen Segmentation*
ESTIMedia 2004 (Workshop on Embedded Systems for Real-Time Multimedia)
6-7. September 2004., Stockholm, Sweden

Péter Szántó, Béla Fehér: *3D Rendering using FPGAs*
VLSI-SOC 2003 - International Conference on Very Large Scale Integration
1-3, December 2003., Darmstadt, Germany

Péter Szántó, Béla Fehér: *Implementing a Programmable Pixel Pipeline in FPGAs*
Second Hungarian Computer Graphics and Geometry Conference
30. June – 1. July, 2003., Budapest, Hungary