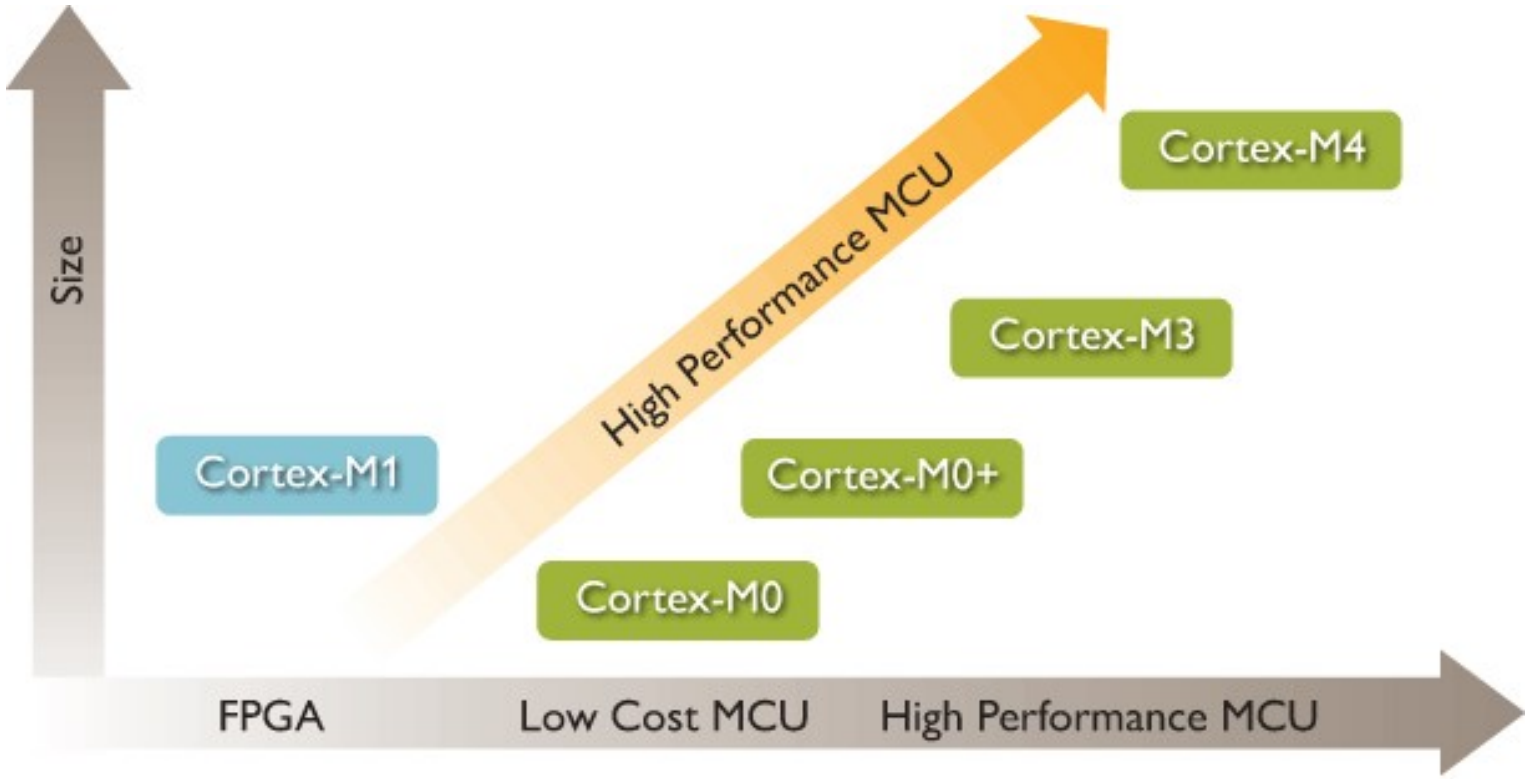
ARM Cortex core microcontrollers
3. Cortex-M0, M4, M7

Scherer Balázs

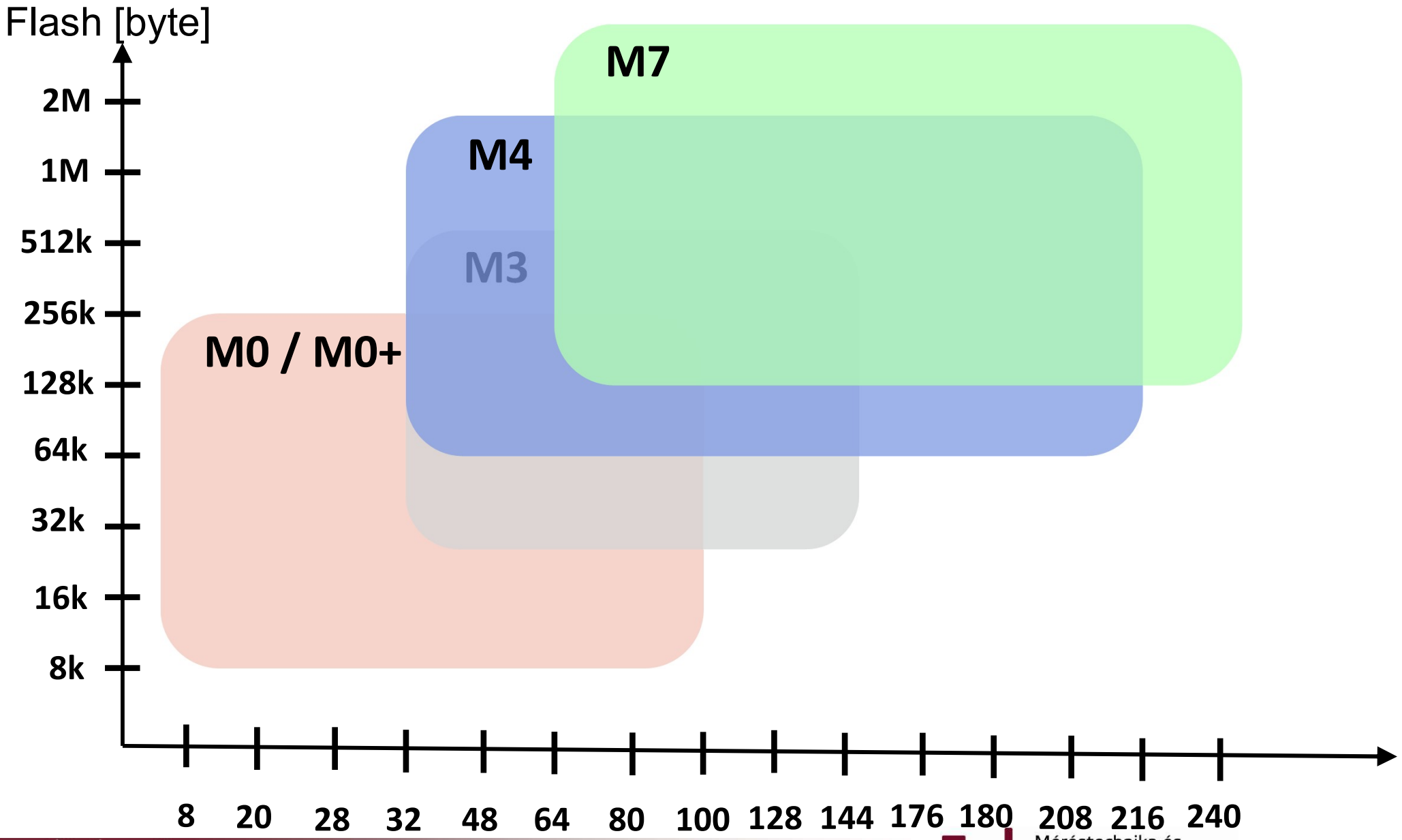
Méréstechnika és
Információs Rendszerek
Tanszék

ARM Cortex-M cores



- M0, M0+: Ultra low power
  - Very simple
  - 85 uW/MHz
- M1: design for FPGA
- M3: General purpose microcontroller
- M4: DSP instructions
- M7: more faster than M4, superscalar, cache

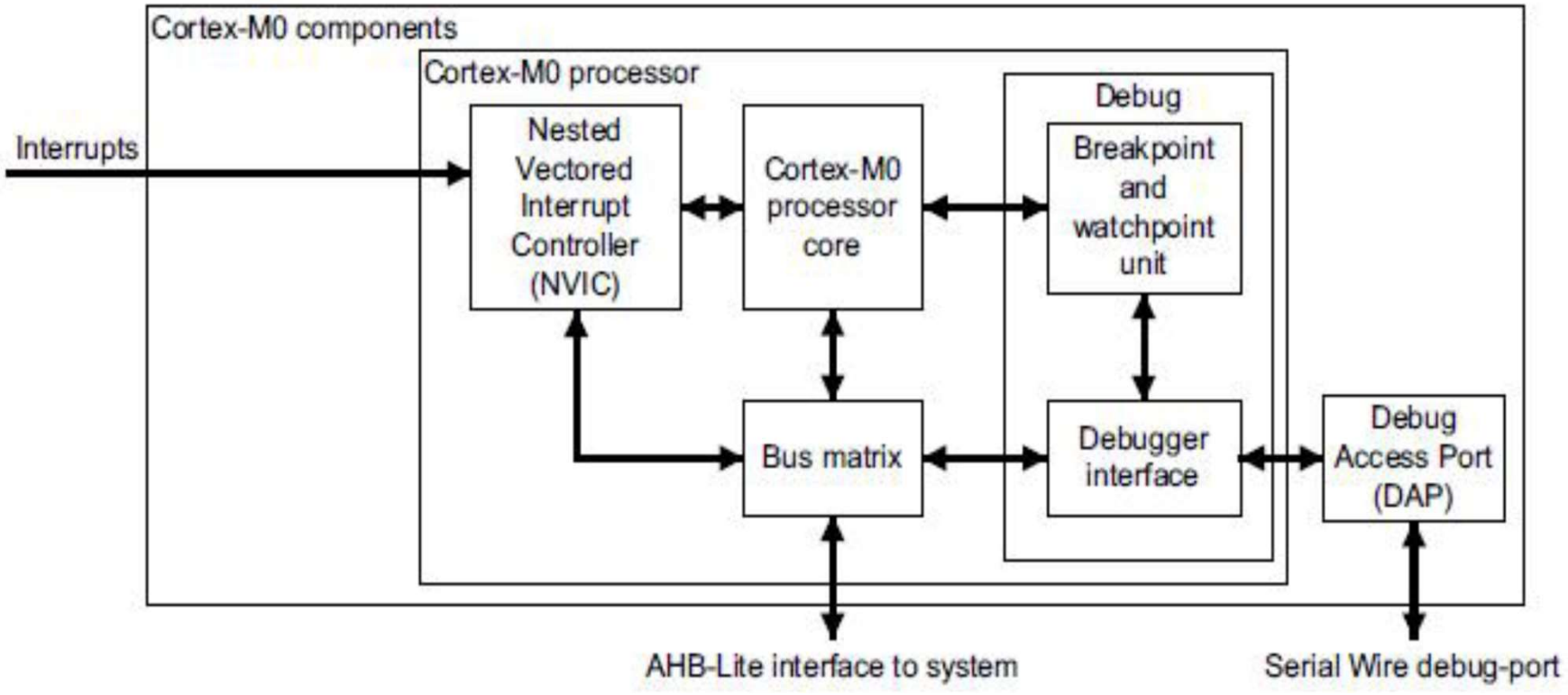
Trends of 32-bit microcontrollers 2003-2024



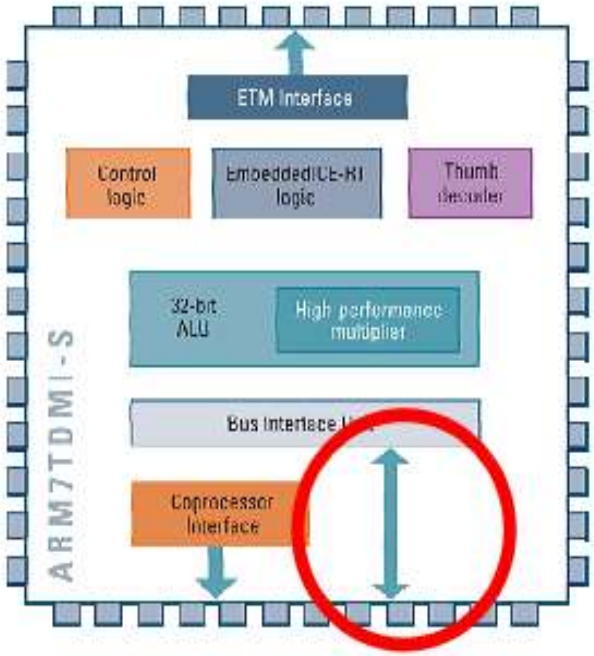
ARM Cortex-M0

A Cortex-M0 core

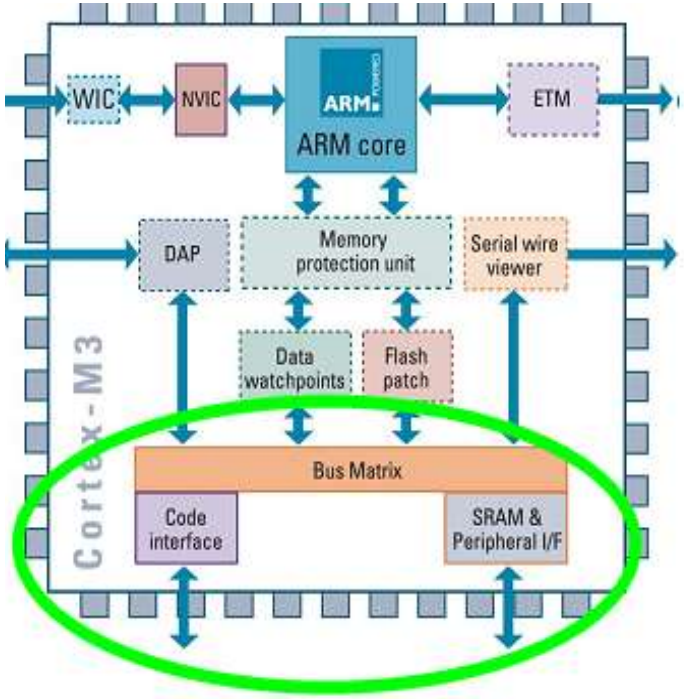
- 32-bit core, 2 stage pipeline
- Neumann architecture
  - Very simple
- ARMv6-M architecture
  - 16-bit Thumb instruction set extended with some Thumb-2 instructions



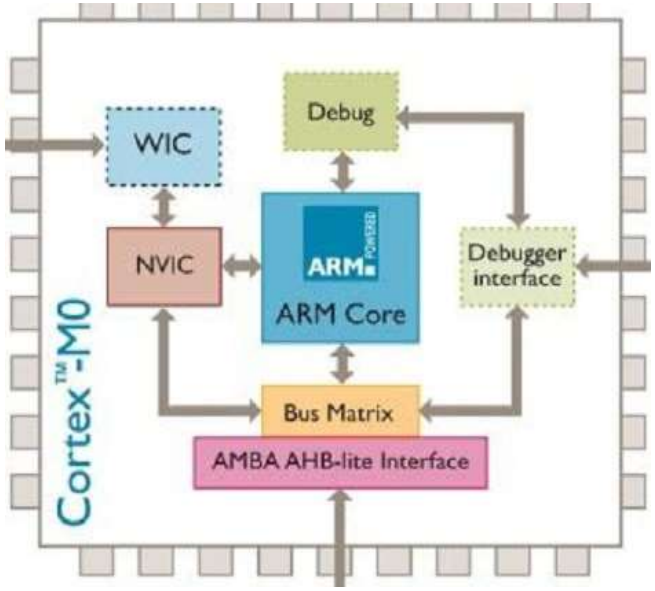
ARM7, Cortex-M3, M0 comparison: bus systems



ARM7TDMI



Cortex-M3



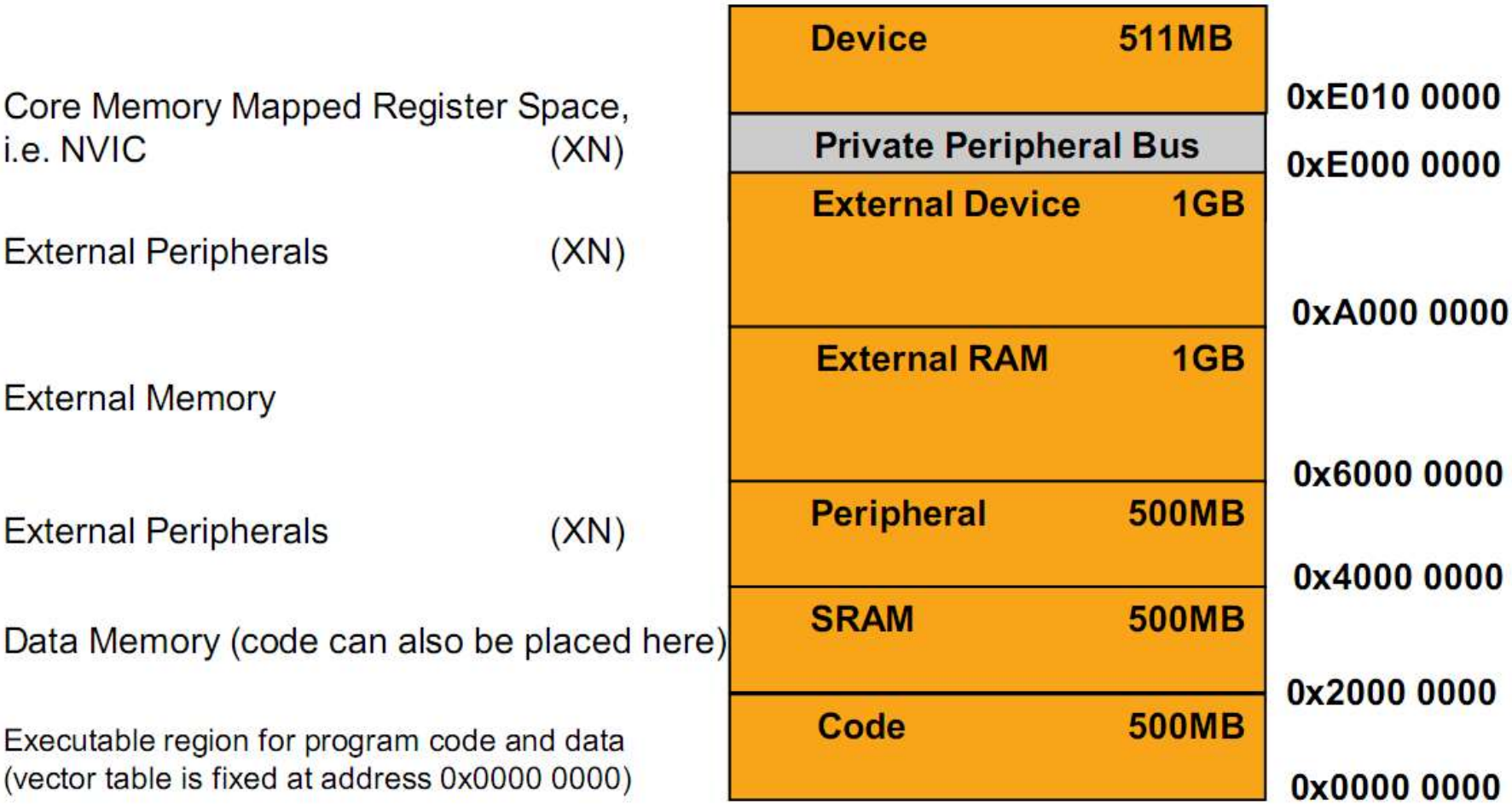
Cortex-M0

Registers

- Similar to other ARM Cortex cores
  - R0 – R3: C subroutine parameters
  - R0 (R1) return values
  - R4 – R11 local register variables
  - R12 Intra-Procedure-call
  - R13 Stack Pointer
  - R14 Link Register
  - R15 Program Counter

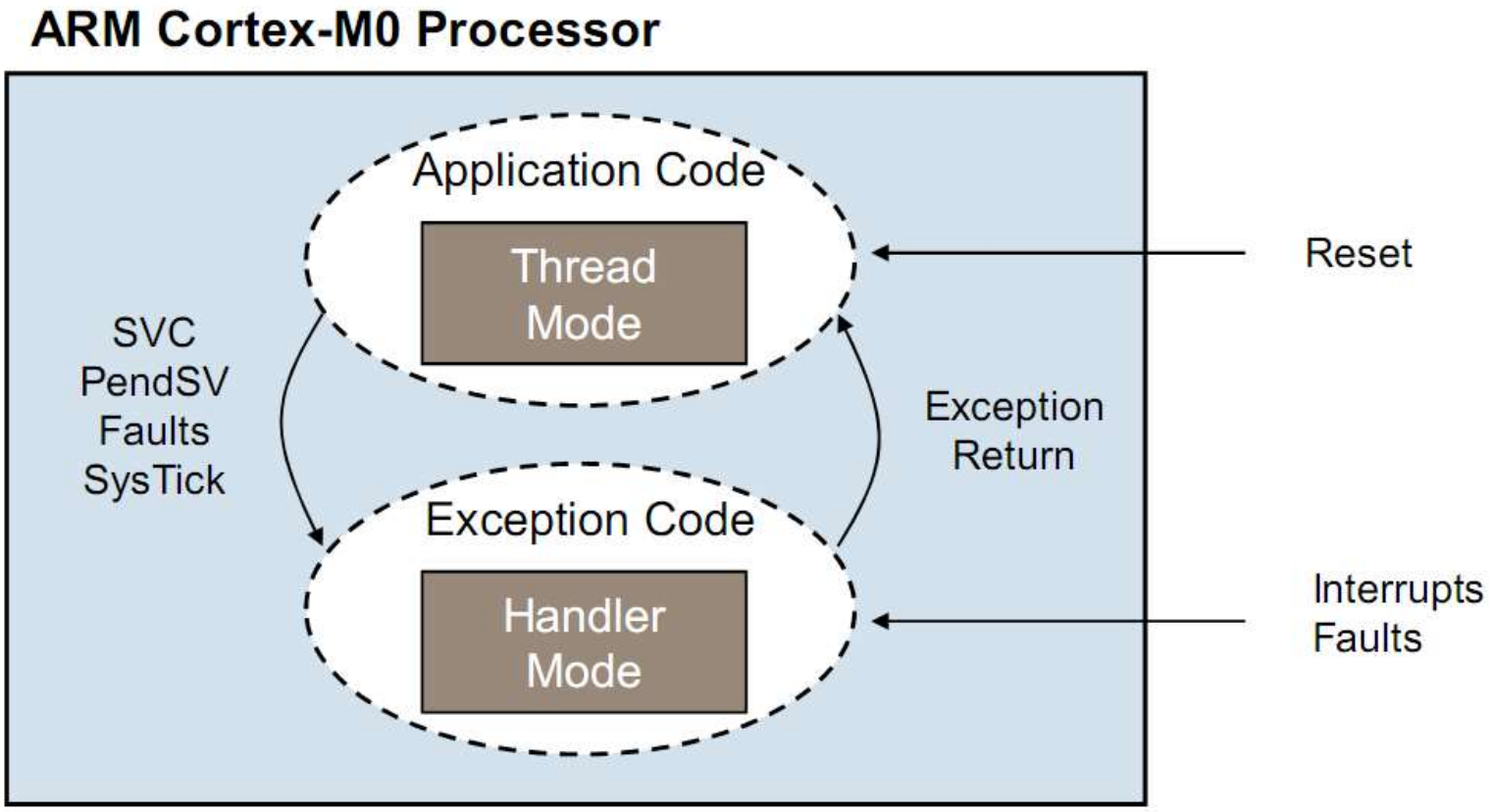
Memory map

- Compatible with M3



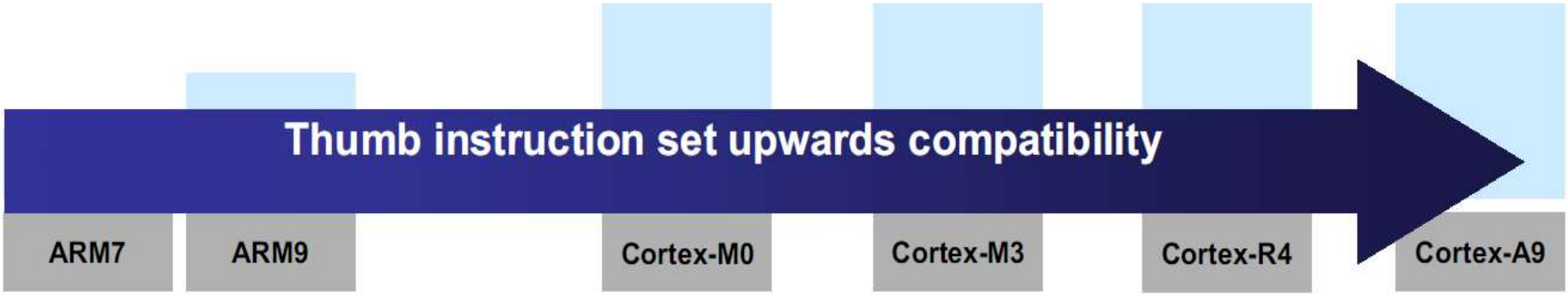
Operation modes

- Same as M3
  - Handler and Thread mode

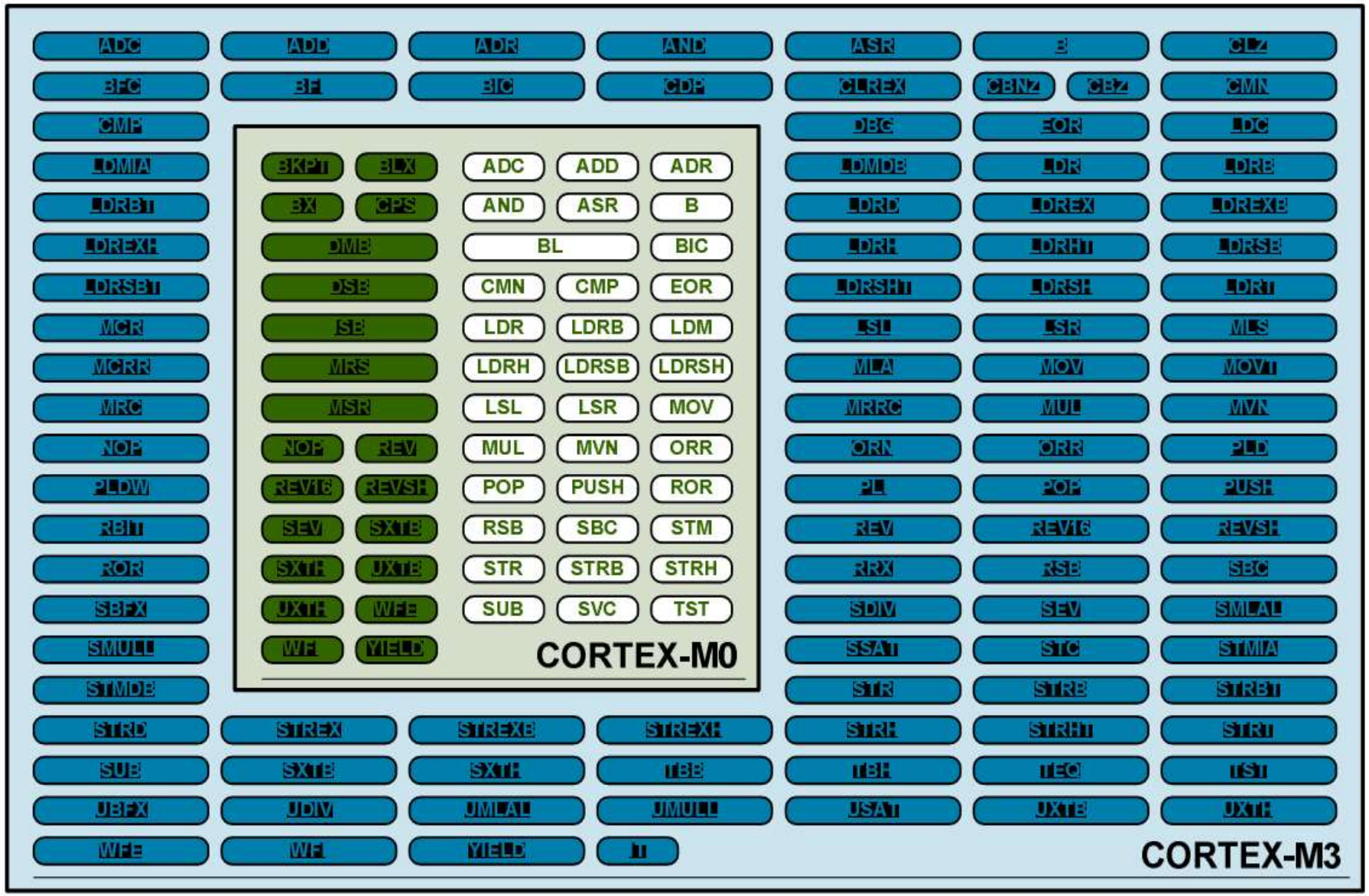


Instruction set

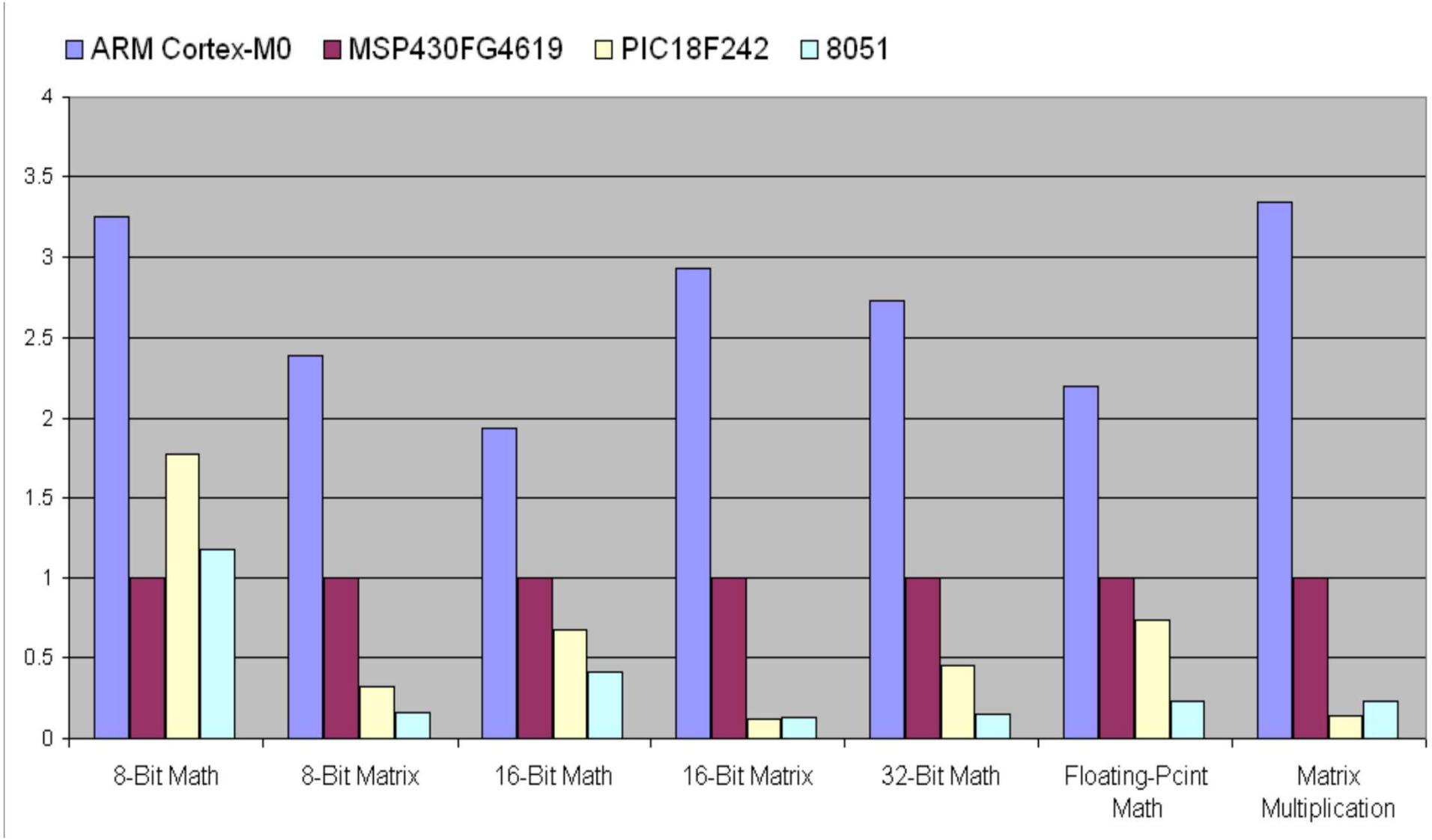
- Thumb-2
  - The modernization of the old Thumb instruction set. Reduced number of instructions 56 pieces. Granted execution speed.
  - The instruction set of Cortex M0 can be used by any other Cortex M core.
  - 0,9 DMIPS/MHz



Cortex-M0 and M3 instruction set comparison

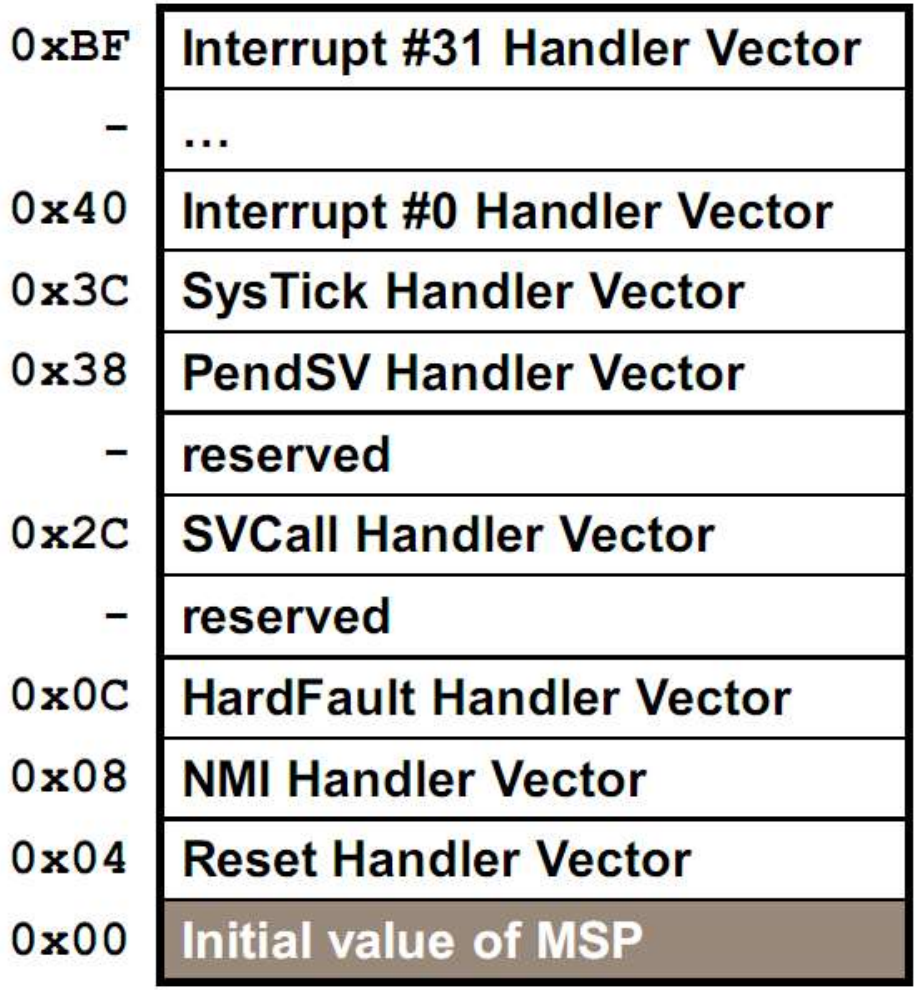


Cortex-M0 core performance



NVIC, Nested Vector Interrupt Controller

- Very Similar to the one in Cortex M3
- Maximum 32 external vectors
- Staring Stack pointer at 0x0
- 4 priority levels



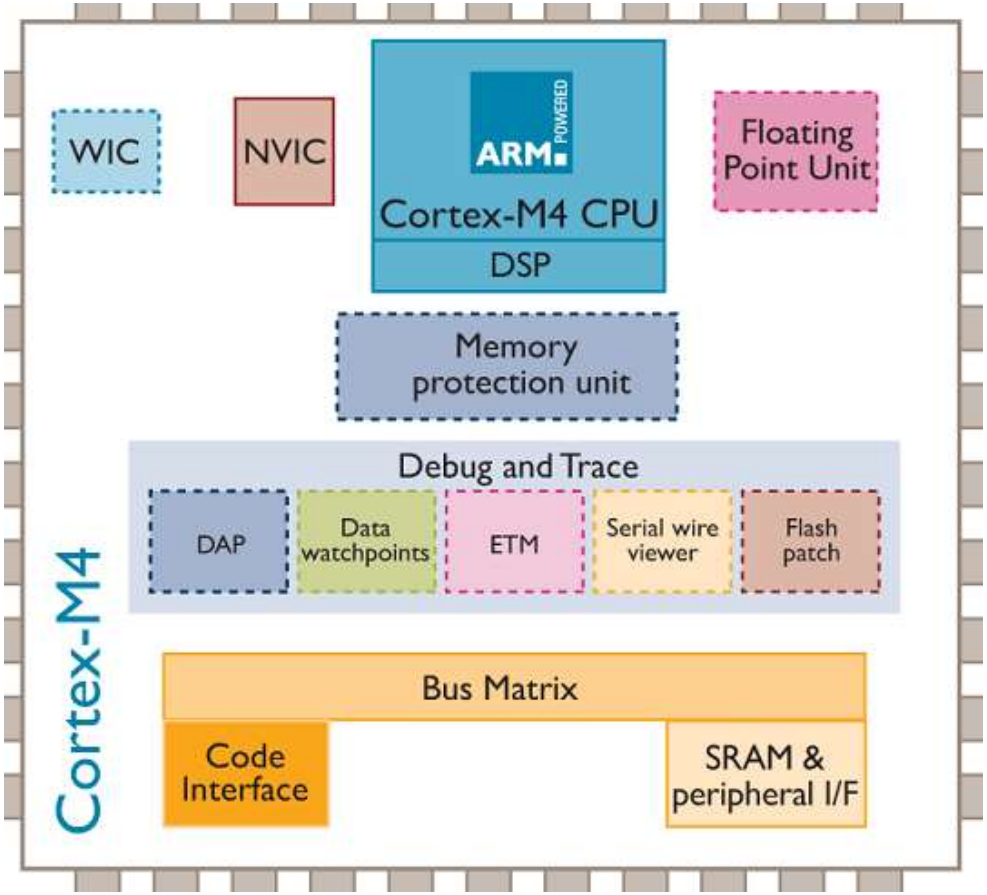
Cotex M0+

- Optimized version of Cortex M0
  - Pipeline reduced to 2 stages
  - Micro Trace Buffer possibility (simplified instruction trace)
  - Optional memory protection unit
  - Optional vector table relocation
  - On clock cycle I/O port handling
  - 13,3 µW/MHz (M0) -> 11,2 µW/MHz (M0+)
    - (32 µW/MHz (M3))

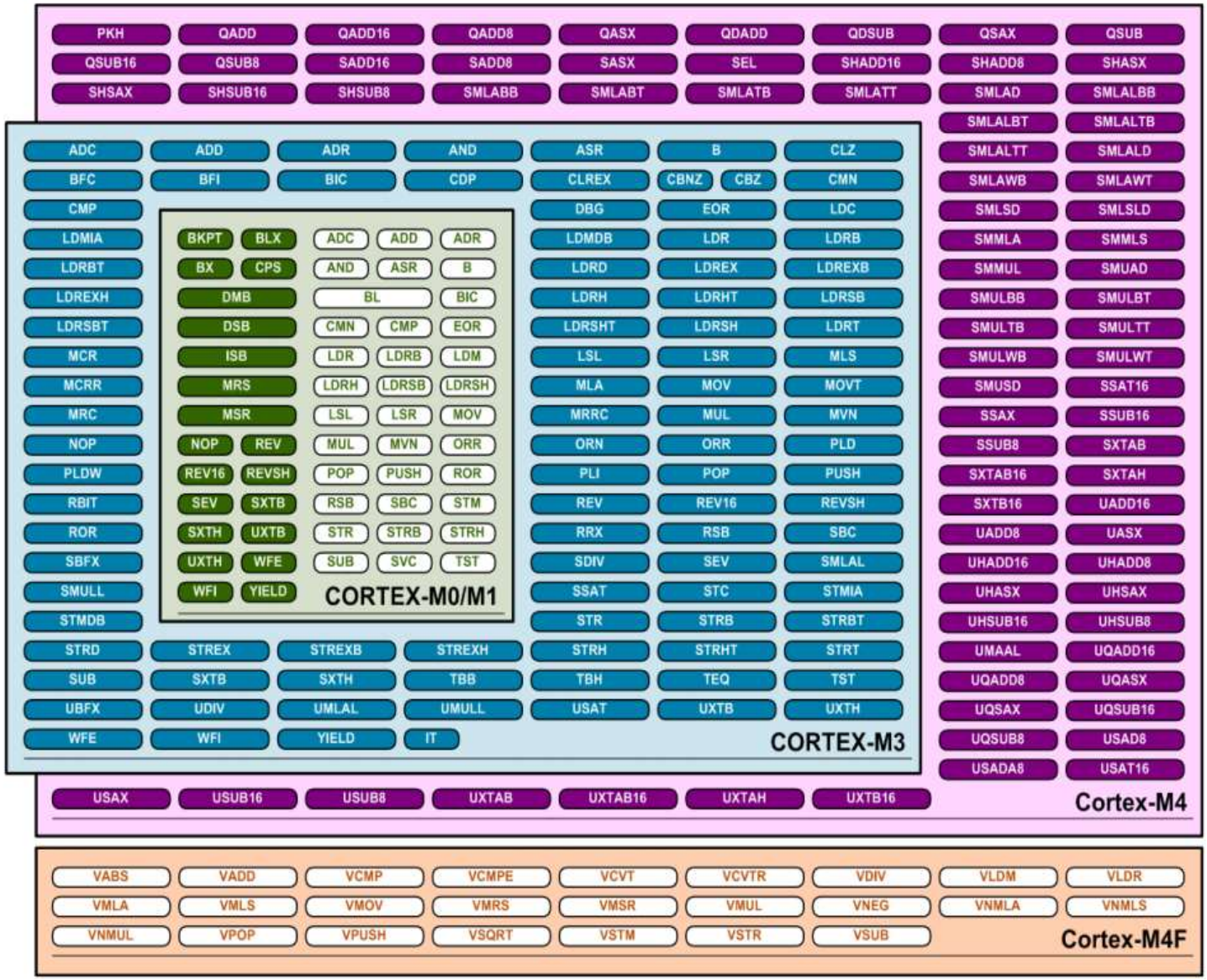
ARM Cortex-M4

Cortex-M4

- Cortex-M4 processor
  - Thumb-2 instruction set
  - DSP and SIMD instructions
  - One clock cycle MAC (32 x 32 + 64 -> 64)
  - Optional single precision FPU
  - Code compatible with M3
- 1,27 / 1,55 / 1,95 DMIPS/MHz
- Architecture
  - 3 phase pipeline with branch prediction
  - 3x AHB-Lite Bus Interface
- Power safe modes
  - Deep Sleep Mode, Wakeup IT
  - Power down options for the FPU
- NVIC (1-240 IT and priority)
- Memory Protection Unit
- Debug & Trace



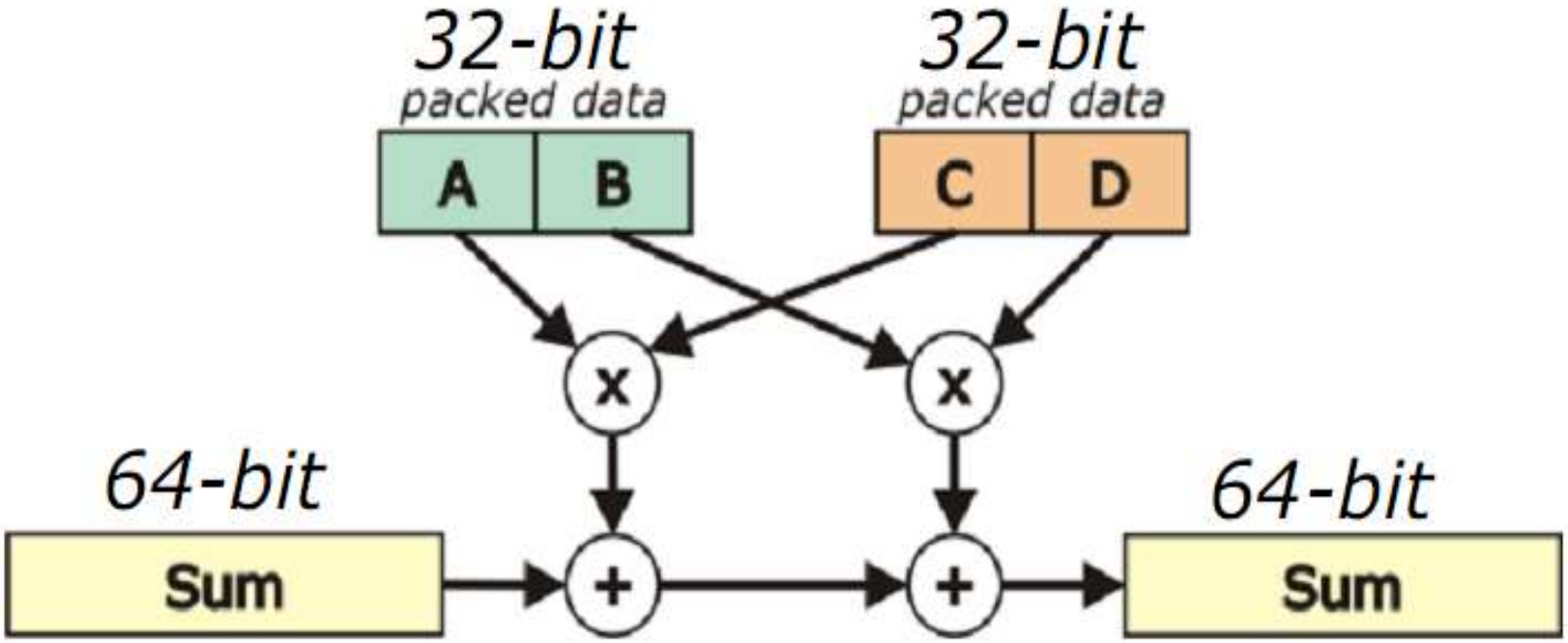
Cortex-M4 instruction set



SIMD (Single Instruction Multiple Data)

- Performing the same operations to many variable in one cycle
- Using compressed 16-bit variables

$$Sum = Sum + (A \times C) + (B \times D)$$



One clock cycle MAC instructions

OPERATION	INSTRUCTION	CYCLES
16 x 16 = 32	SMULBB, SMULBT, SMULTB, SMULTT	1
16 x 16 + 32 = 32	SMLABB, SMLABT, SMLATB, SMLATT	1
16 x 16 + 64 = 64	SMLALBB, SMLALBT, SMLALTB, SMLALTT	1
16 x 32 = 32	SMULWB, SMULWT	1
(16 x 32) + 32 = 32	SMLAWB, SMLAWT	1
(16 x 16) ± (16 x 16) = 32	SMUAD, SMUADX, SMUSD, SMUSDX	1
(16 x 16) ± (16 x 16) + 32 = 32	SMLAD, SMLADX, SMLSD, SMLSDX	1
(16 x 16) ± (16 x 16) + 64 = 64	SMLALD, SMLALDX, SMLSLD, SMLSLDX	1
32 x 32 = 32	MUL	1
32 ± (32 x 32) = 32	MLA, MLS	1
32 x 32 = 64	SMULL, UMULL	1
(32 x 32) + 64 = 64	SMLAL, UMLAL	1
(32 x 32) + 32 + 32 = 64	UMAAL	1
32 ± (32 x 32) = 32 (upper)	SMMLA, SMMLAR, SMMLS, SMMLSR	1
(32 x 32) = 32 (upper)	SMMUL, SMMULR	1

Cortex-M4 instruction set

		Cycle counts		
CLASS	INSTRUCTION	ARM9E-S	CORTEX-M3	Cortex-M4
Arithmetic	ALU operation (not PC)	1 - 2	1	1
	ALU operation to PC	3 - 4	3	3
	CLZ	1	1	1
	QADD, QDADD, QSUB, QDSUB	1 - 2	n/a	1
	QADD8, QADD16, QSUB8, QSUB16	n/a	n/a	1
	QDADD, QDSUB	n/a	n/a	1
	QASX, QSAX, SASX, SSAX	n/a	n/a	1
	SHASX, SHSAX, UHASX, UHSAX	n/a	n/a	1
	SADD8, SADD16, SSUB8, SSUB16	n/a	n/a	1
	SHADD8, SHADD16, SHSUB8, SHSUB16	n/a	n/a	1
	UQADD8, UQADD16, UQSUB8, UQSUB16	n/a	n/a	1
	UHADD8, UHADD16, UHSUB8, UHSUB16	n/a	n/a	1
	UADD8, UADD16, USUB8, USUB16	n/a	n/a	1
	UQASX, UQSAX, USAX, UASX	n/a	n/a	1
	UXTAB, UXTAB16, UXTAH	n/a	n/a	1
	USAD8, USADA8	n/a	n/a	1
Multiplication	MUL, MLA	2 - 3	1 - 2	1
	MULS, MLAS	4	1 - 2	1
	SMULL, UMULL, SMLAL, UMLAL	3 - 4	5 - 7	1
	SMULBB, SMULBT, SMULTB, SMULTT	1 - 2	n/a	1
	SMLABB, SMLBT, SMLATB, SMLATT	1 - 2	n/a	1
	SMULWB, SMULWT, SMLAWB, SMLAWT	1 - 2	n/a	1
	SMLALBB, SMLALBT, SMLALTB, SMLALTT	2 - 3	n/a	1
	SMLAD, SMLADX, SMLALD, SMLALDX	n/a	n/a	1
	SMLSD, SMLSDX	n/a	n/a	1
	SMLSLD, SMLSLD	n/a	n/a	1
	SMMLA, SMMLAR, SMMLS, SMMLSR	n/a	n/a	1
	SMMUL, SMMULR	n/a	n/a	1
	SMUAD, SMUADX, SMUSD, SMUSDX	n/a	n/a	1
	UMAAL	n/a	n/a	1
Division	SDIV, UDIV	n/a	2 - 12	2 - 12

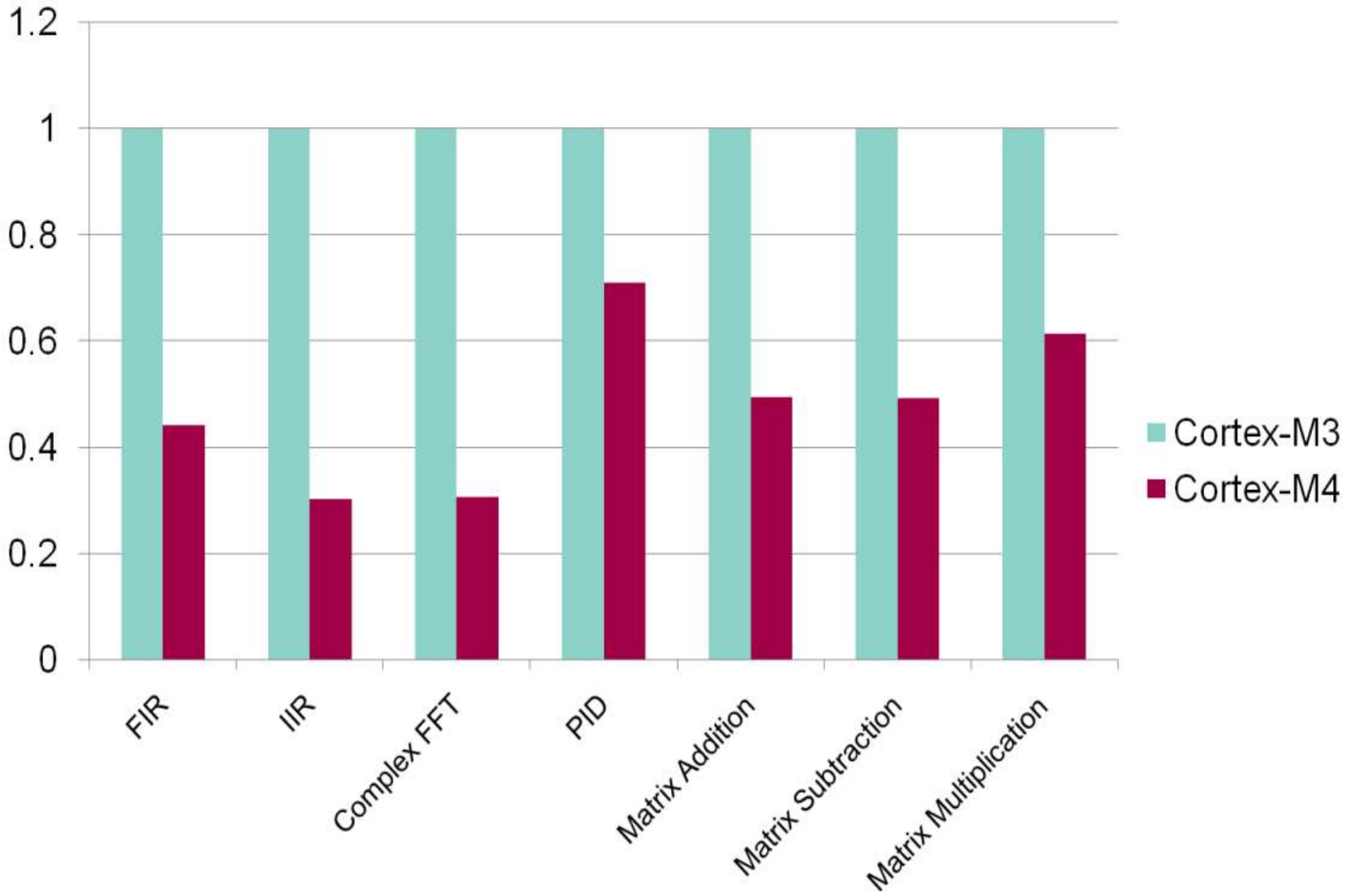
Single cycle MAC

Cortex-M4 FIR filter

- Using a DSP with assembly code: 1 cycle
- Cortex-M4 standard C code: 12 cycle
- Optimized C code: 6 cycle
- Assembly using SIMD instructions to 16-bit variables: 2-3 cycles
- Optimized assembly code 1,5-2 cycle

- Nearly the same performance as a DSP.

Cortex-M3, M4 comparison: 16-bit arithmetic



Foating point unit

- IEEE 754 standard based
- Capabilities:

OPERATION	CYCLE COUNT
Add/Subtract	1
Divide	14
Multiply	1
Multiply Accumulate (MAC)	3
Fused MAC	3
Square Root	14

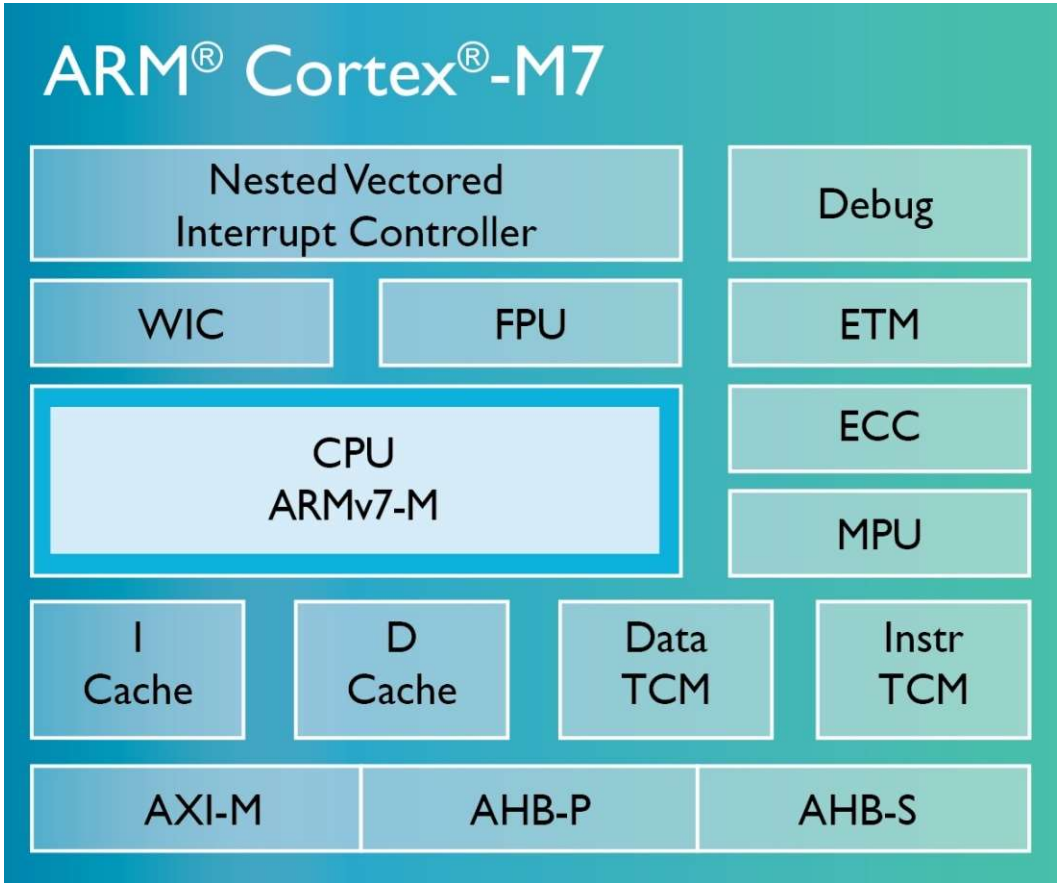
DSP Library support

- CMSIS DSP library
  - Basic mathematic operations: vector operations
  - Trigonometrical operations: sin, cos, sqrt stb.
  - Interpolation: linear, bilinear
  - Complex math:
    - Statistics: max, min, RMS etc.
    - Filtering: IIR, FIR, LMS etc.
    - Transformations: FFT
    - Matrix operations
    - PID controller

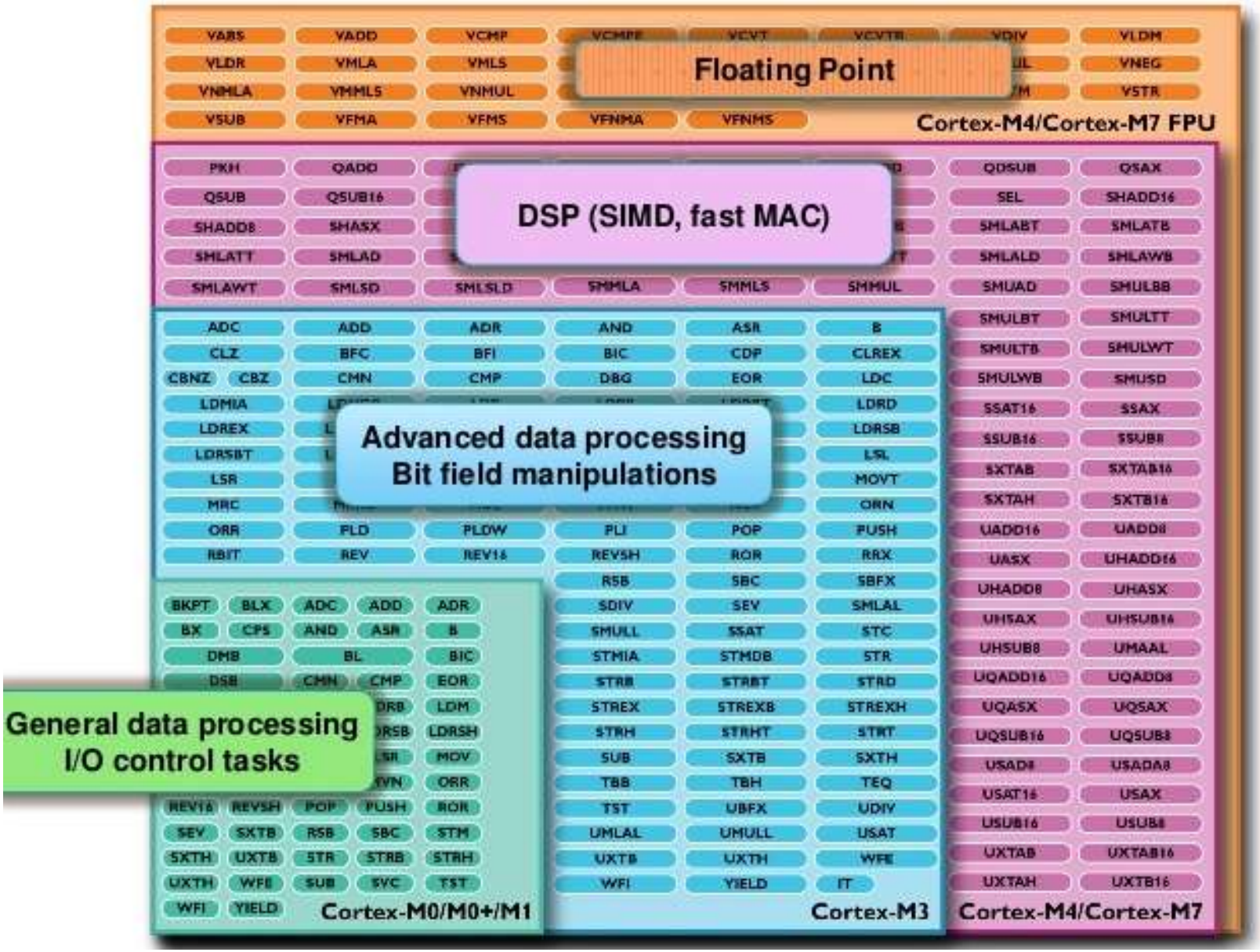
ARM Cortex-M7

Cortex-M7

- ARMv7-M architecture
- Built-in Floating point unit
- 6 stage pipeline
  - superscalar
  - branch prediction
- 2,14 – 3,23 DMIPS/MHz
- 0 – 64 kB 2 way instruction cache
- 0 – 64kB 4 way data cache
- 8 or 16 region MPU
- ECC Error correcting code
- Lock-step possibility

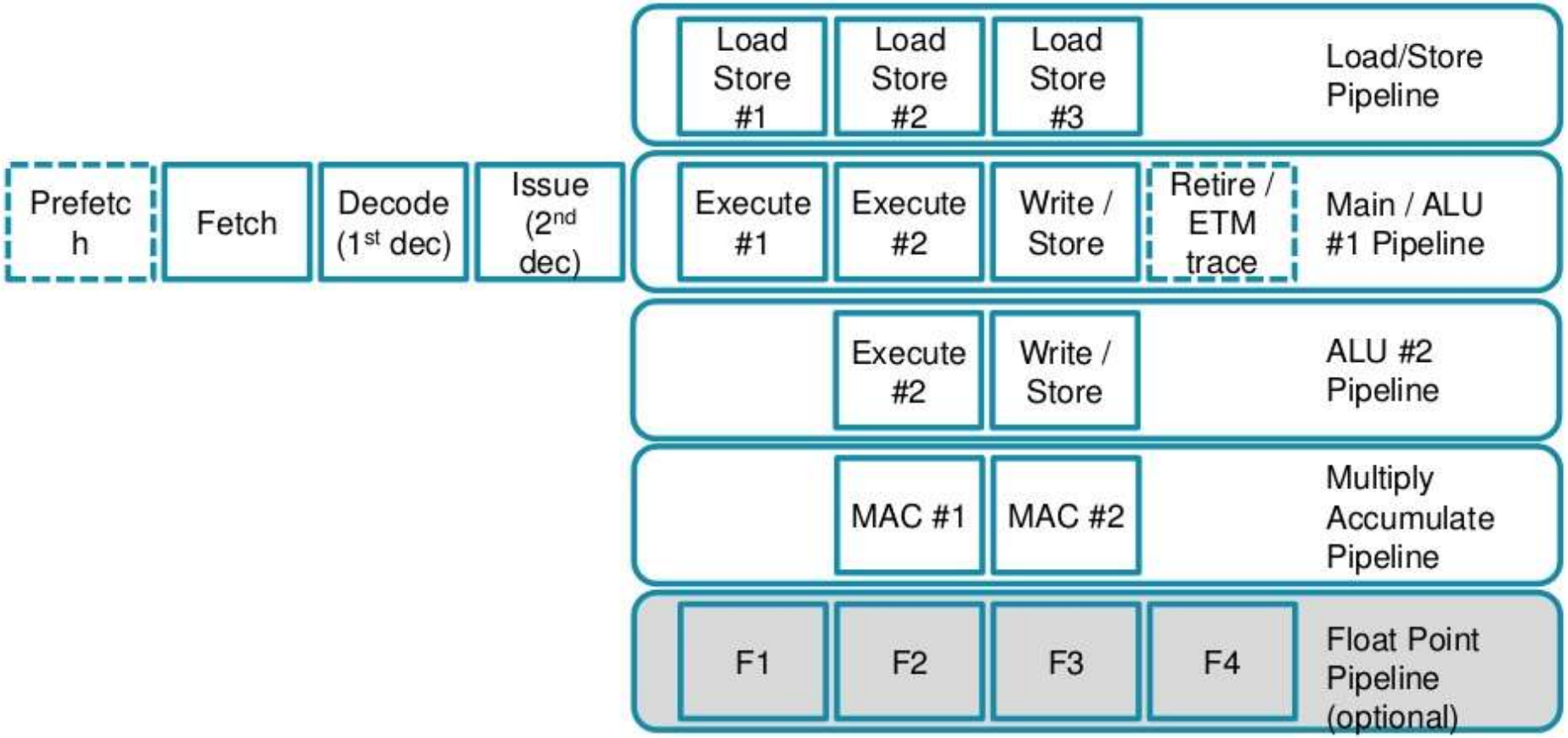


M7 instruction set



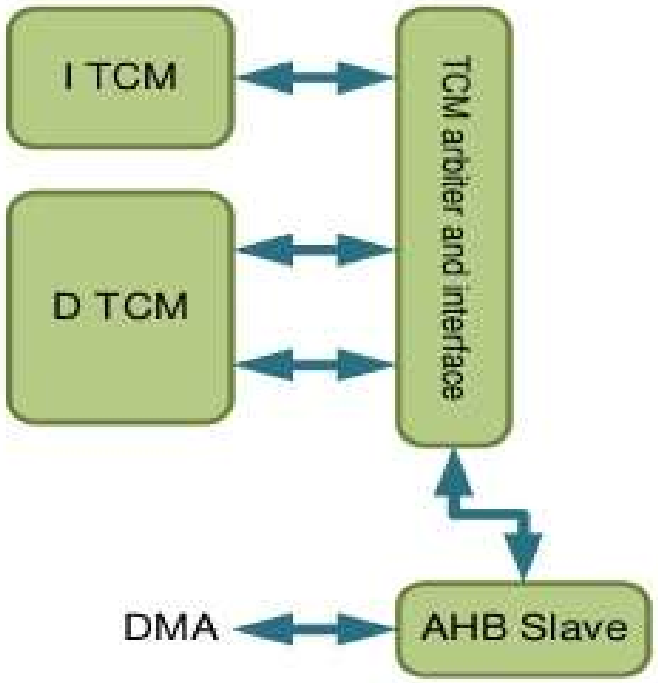
M7 pipeline

- 6 stage superscalar pipeline
  - Two shifter, ALU
  - One MAC
  - One floating point pipe

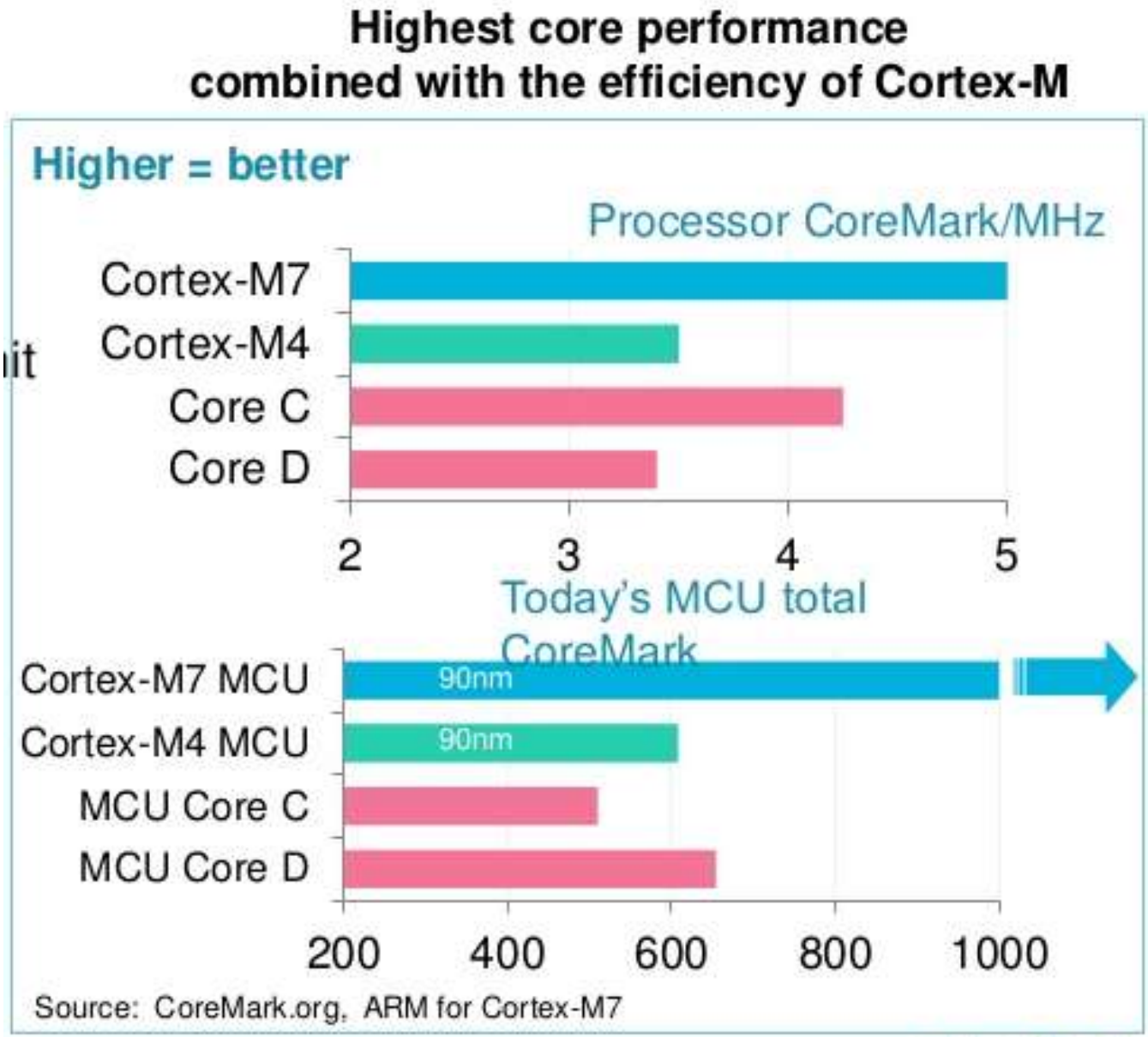


Tightly-coupled memory (TCM)

- Small latency memory, used for predictable, and real-time critical code. Do not have the unpredictability like the cache.
- 16 Mbyte both for instruction and data (instruction 64-bit bus, data 2x32-bit bus).

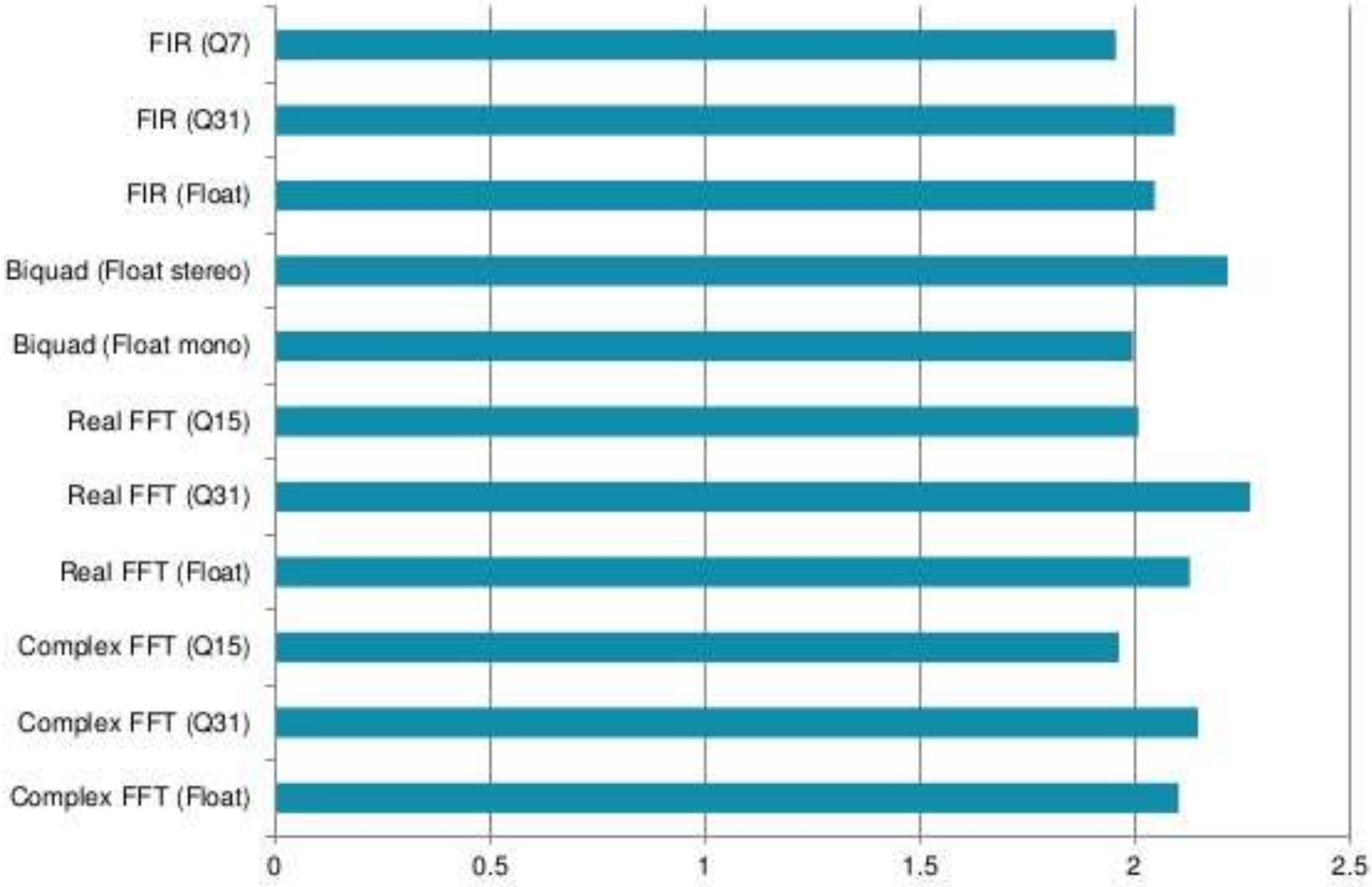


Performance of Cortex M7



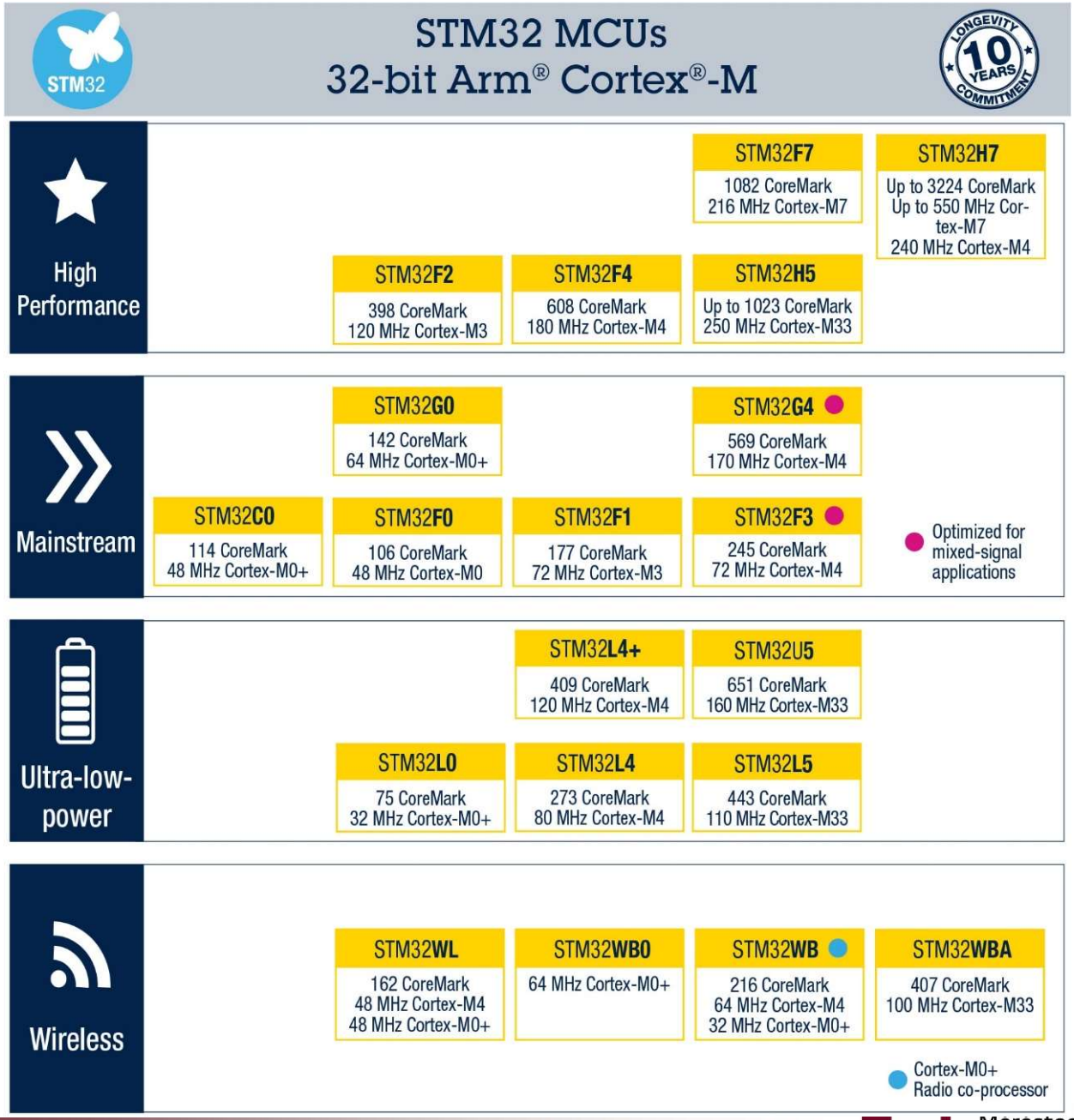
DSP functionality

- Comparing to M4
- CMSIS library support

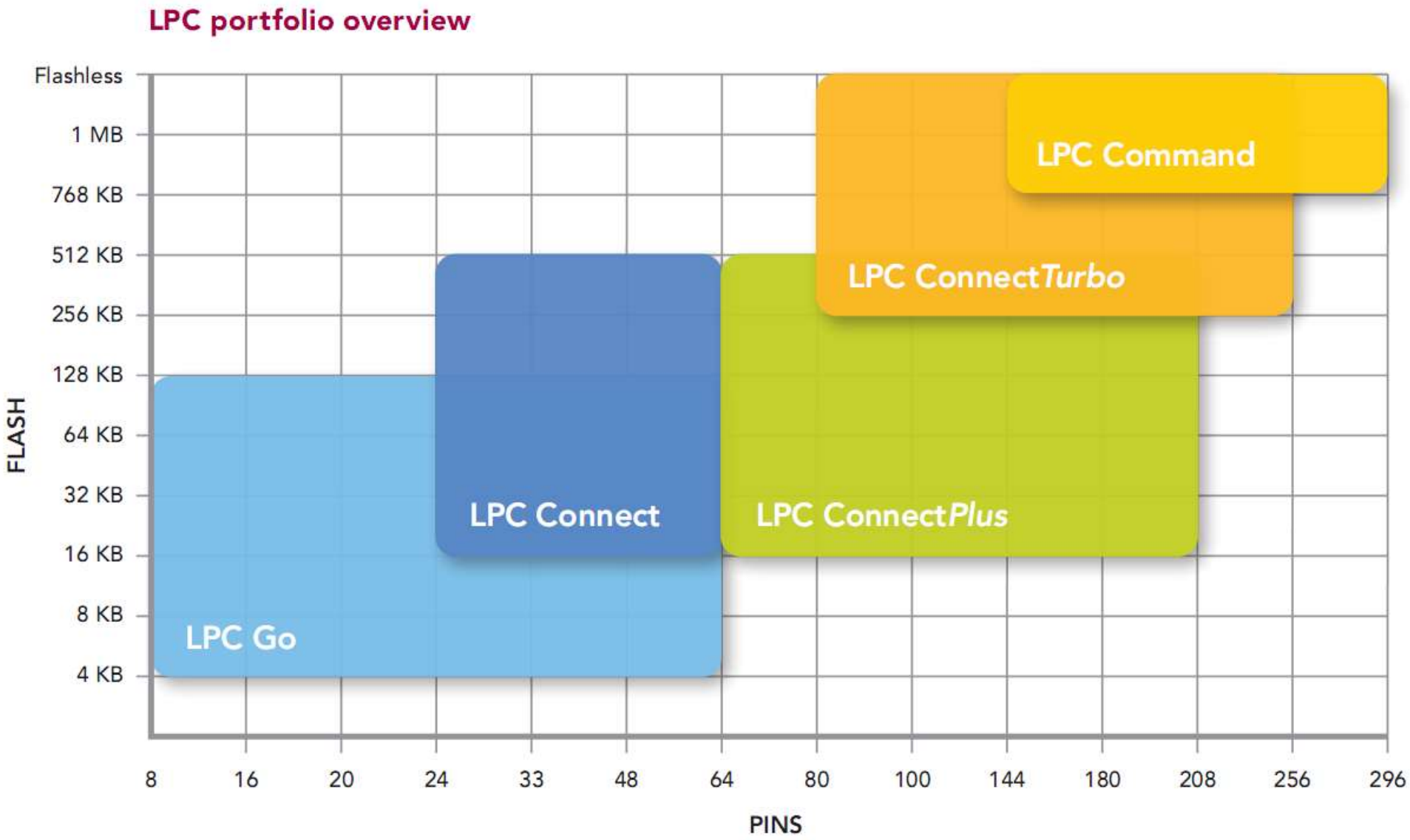


Microcontrollers on the market

ST lines

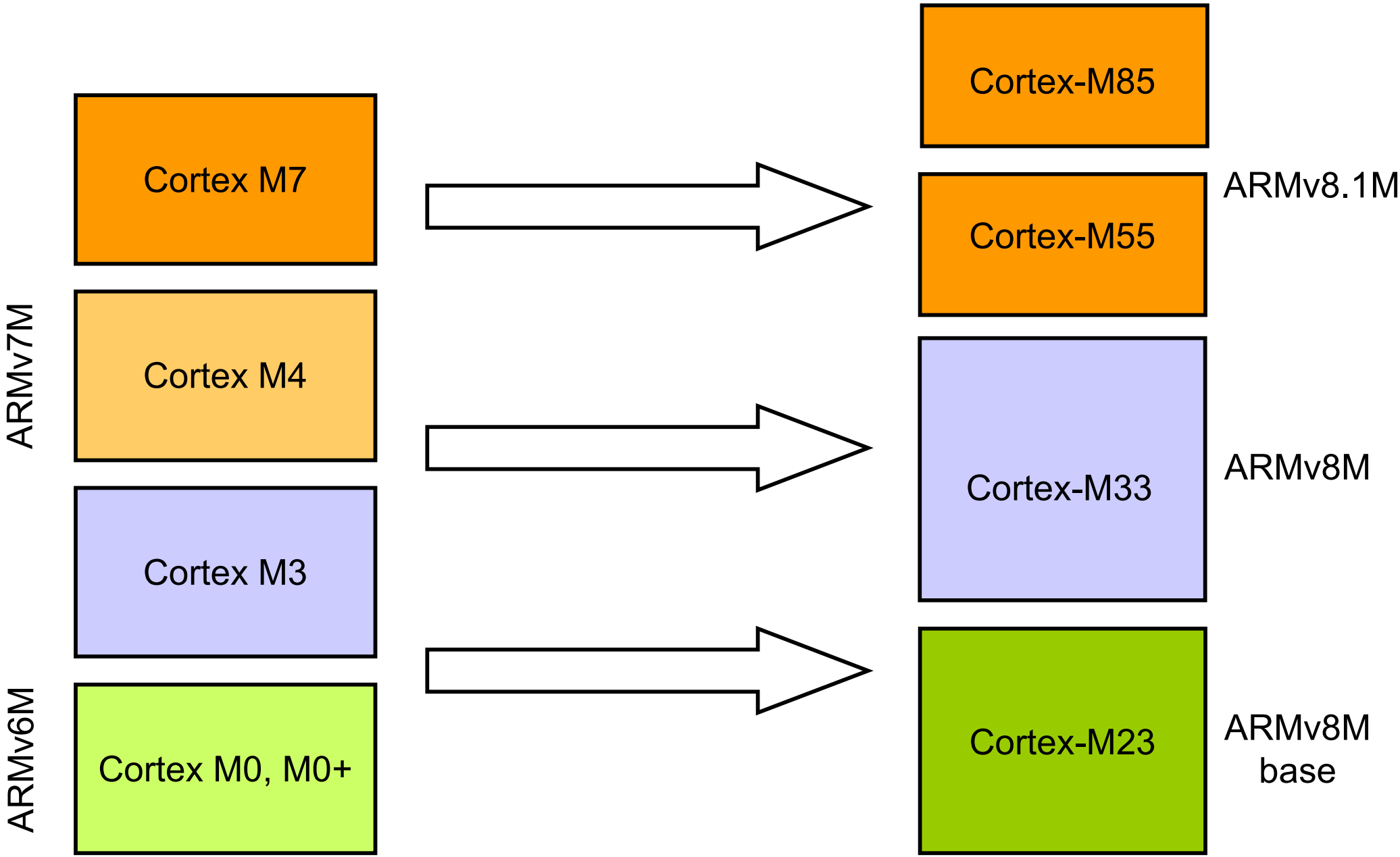

STM32 MCUs
32-bit Arm® Cortex®-M
LONGEVITY 10 YEARS COMMITMENT
High Performance
STM32F7
1082 CoreMark
216 MHz Cortex-M7
STM32H7
Up to 3224 CoreMark
Up to 550 MHz Cortex-M7
240 MHz Cortex-M4
STM32F2
398 CoreMark
120 MHz Cortex-M3
STM32F4
608 CoreMark
180 MHz Cortex-M4
STM32H5
Up to 1023 CoreMark
250 MHz Cortex-M33
Mainstream
STM32G0
142 CoreMark
64 MHz Cortex-M0+
STM32G4
569 CoreMark
170 MHz Cortex-M4
STM32C0
114 CoreMark
48 MHz Cortex-M0+
STM32F0
106 CoreMark
48 MHz Cortex-M0
STM32F1
177 CoreMark
72 MHz Cortex-M3
STM32F3
245 CoreMark
72 MHz Cortex-M4
Optimized for mixed-signal applications
Ultra-low-power
STM32L4+
409 CoreMark
120 MHz Cortex-M4
STM32U5
651 CoreMark
160 MHz Cortex-M33
STM32L0
75 CoreMark
32 MHz Cortex-M0+
STM32L4
273 CoreMark
80 MHz Cortex-M4
STM32L5
443 CoreMark
110 MHz Cortex-M33
Wireless
STM32WL
162 CoreMark
48 MHz Cortex-M4
48 MHz Cortex-M0+
STM32WB0
64 MHz Cortex-M0+
STM32WB
216 CoreMark
64 MHz Cortex-M4
32 MHz Cortex-M0+
STM32WBA
407 CoreMark
100 MHz Cortex-M33
Cortex-M0+ Radio co-processor

NXP lines


LPC portfolio overview
Flashless
1 MB
768 KB
512 KB
256 KB
128 KB
64 KB
32 KB
16 KB
8 KB
4 KB
FLASH
LPC Command
LPC ConnectTurbo
LPC Connect
LPC ConnectPlus
LPC Go
8
16
20
24
33
48
64
80
100
144
180
208
256
296
PINS

New Cortex M cores

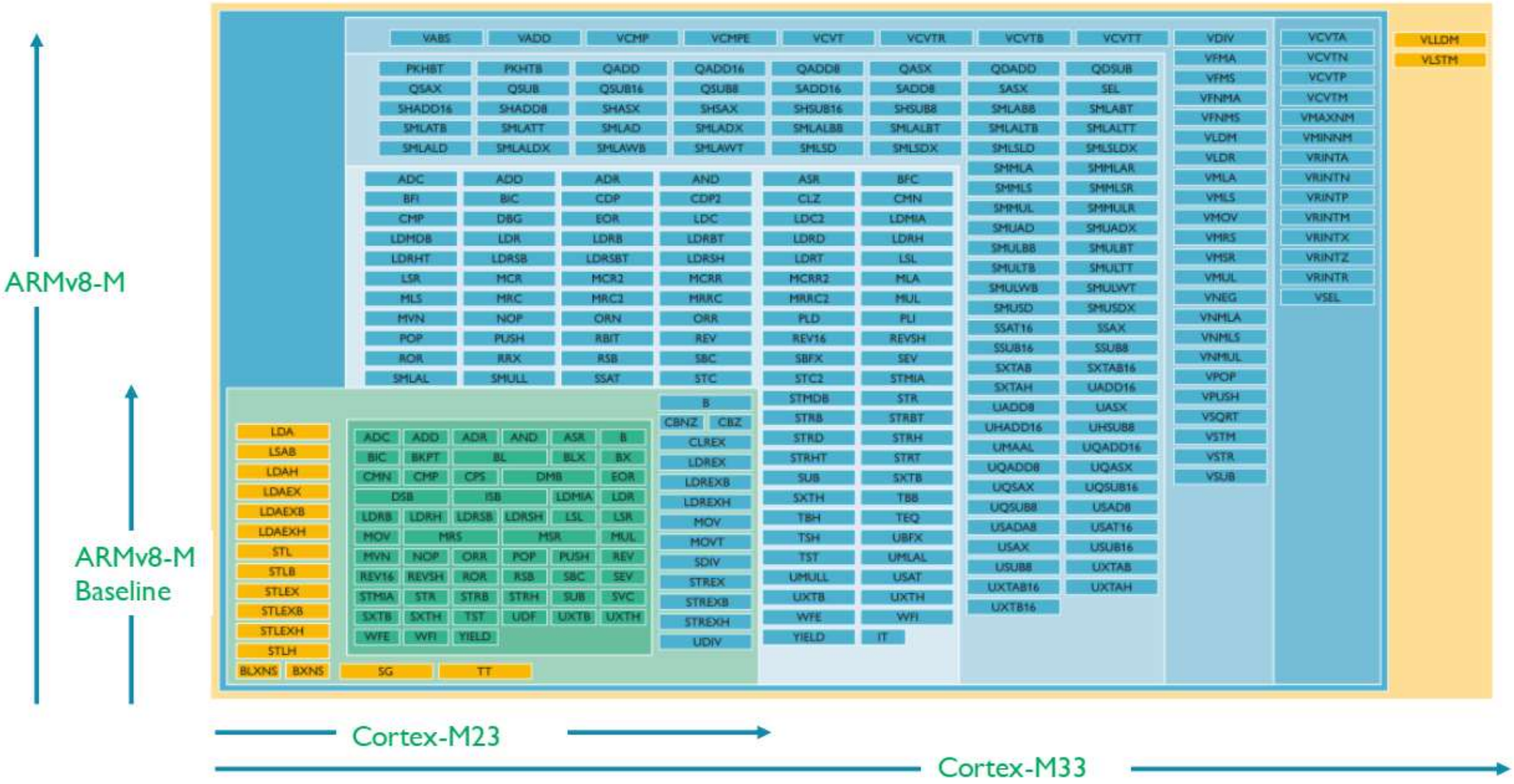
Migration plan for new cores



ARMv8M architecture features

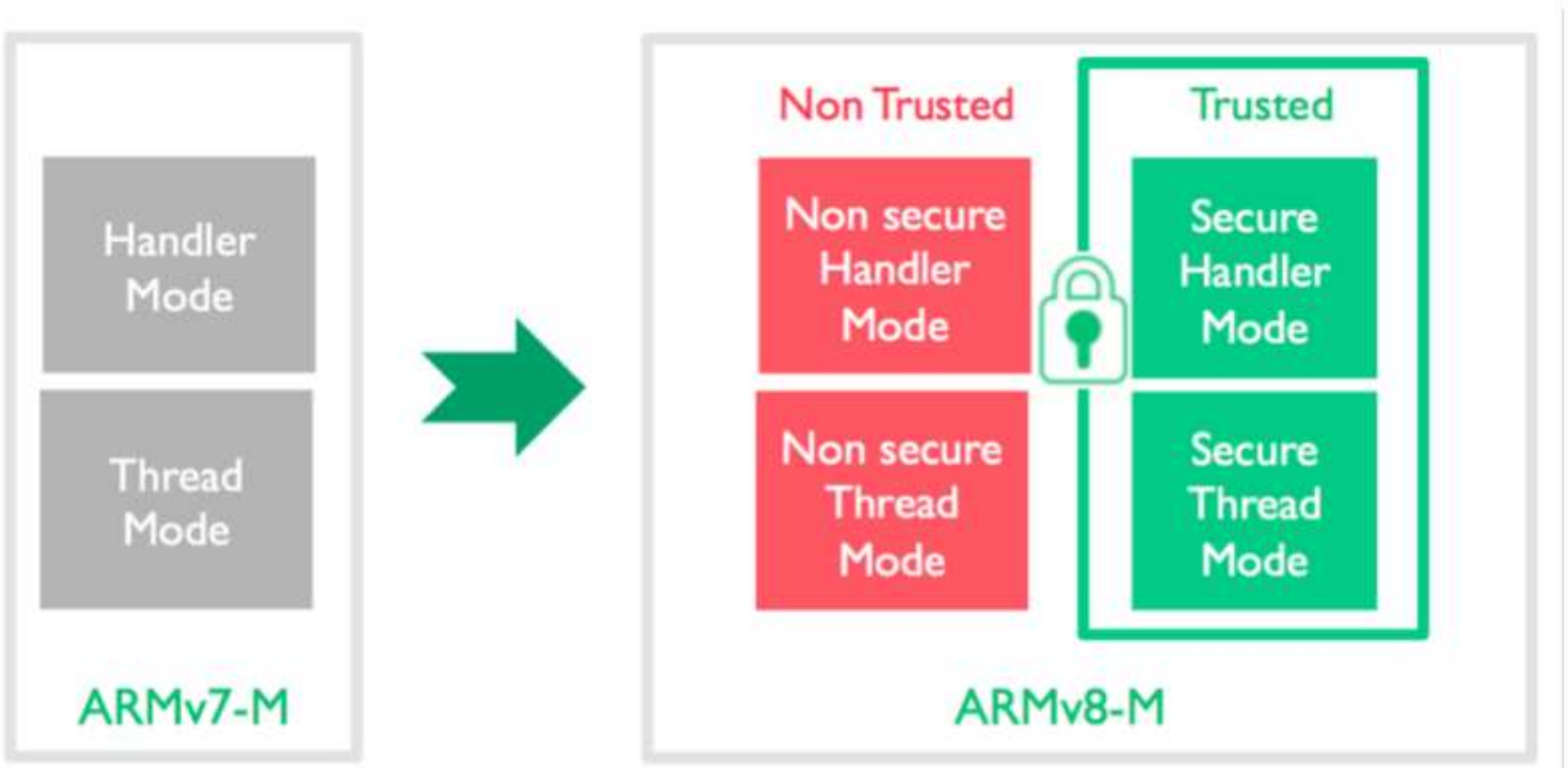
- Stack limit registers
  - Hardware checking for stack overflow
- Syncronization support
  - LOAD Exlusive
  - STORE Exlusive
- No bit-band
- Trust Zone
  - Barrier between secure code parts, and non secure code parts

ARMv8M instruction set



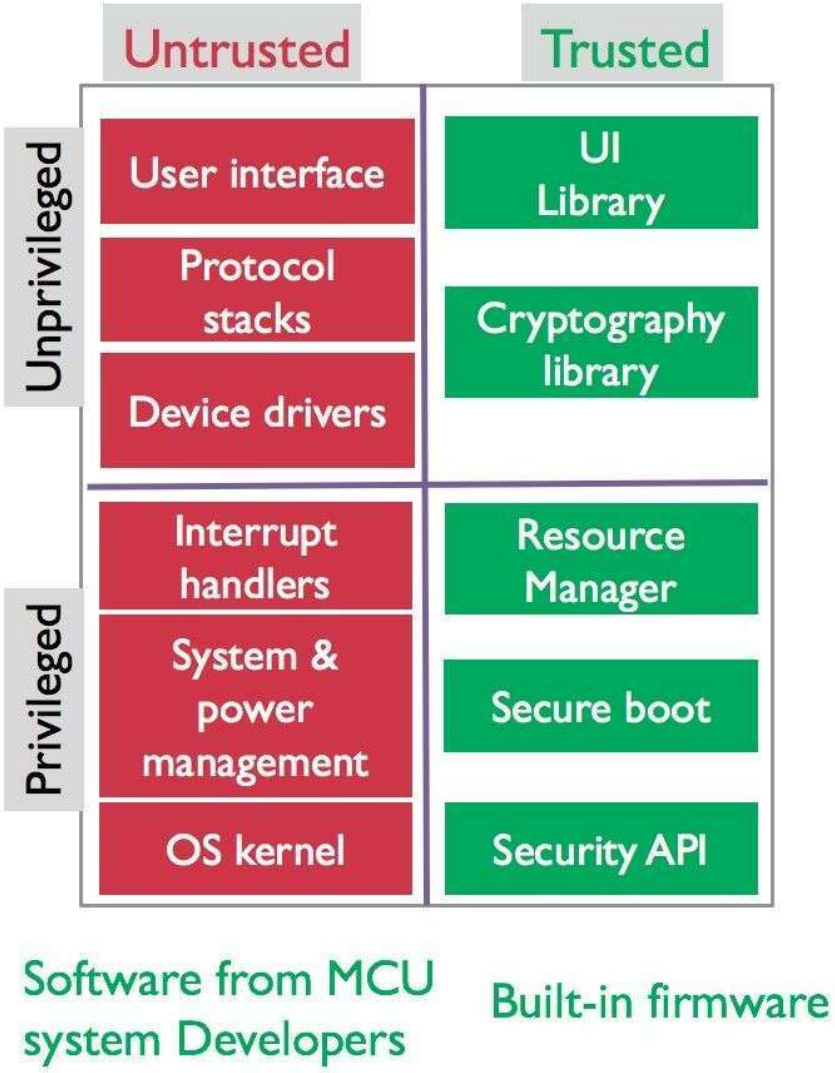
Trust Zone

- Separation of memory into Secure and non-Secure, more advanced separation than Memory Protection Unit
- Separate banked stack pointers for secure mode
- Separate secure, non secure IT table options

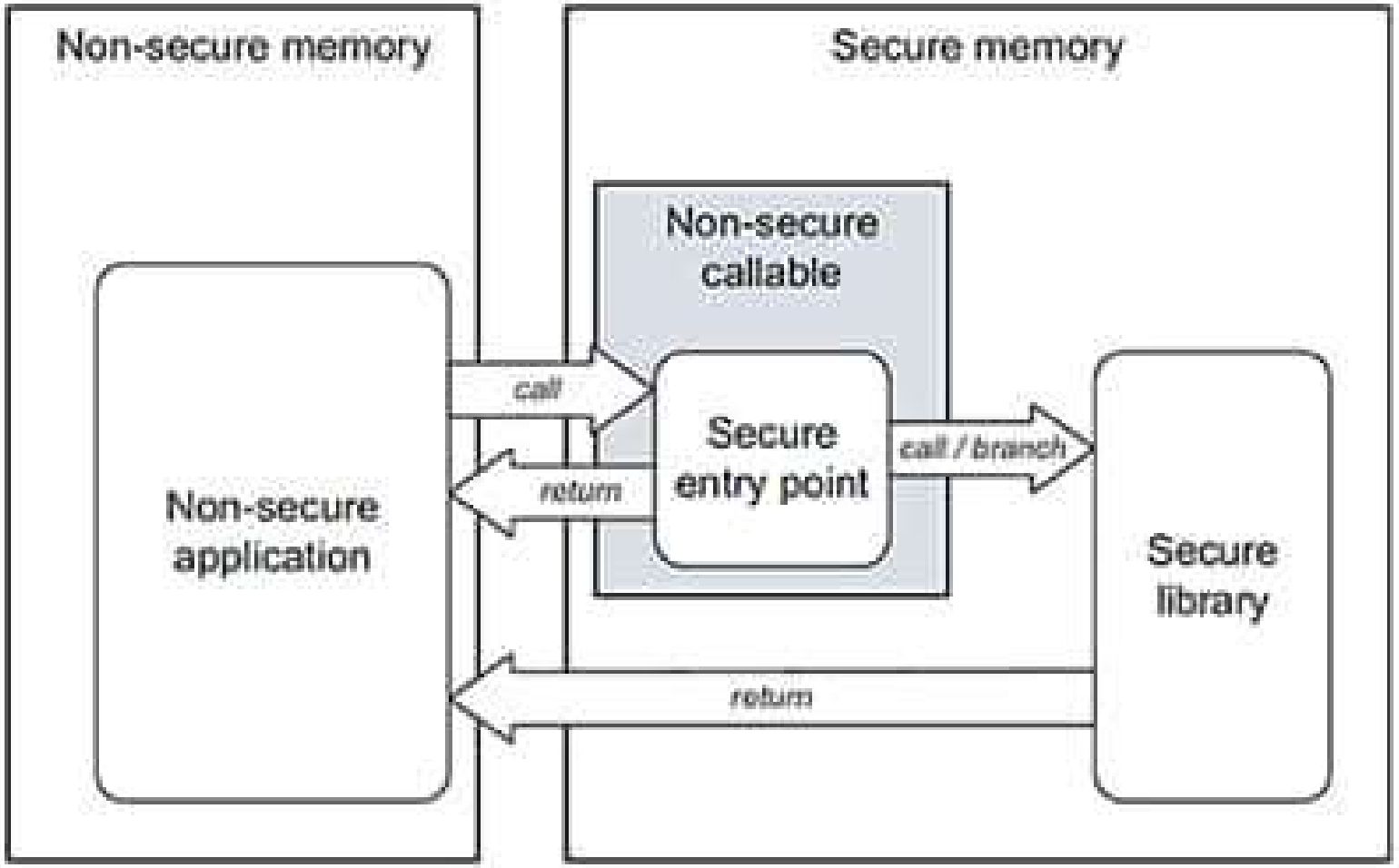


Typical usage of Trust Zone

- Anything that can be put into Trusted territory that is not allowed to be changed or read by the user code
  - Licensed software stack
  - Encryption keys and algorithms

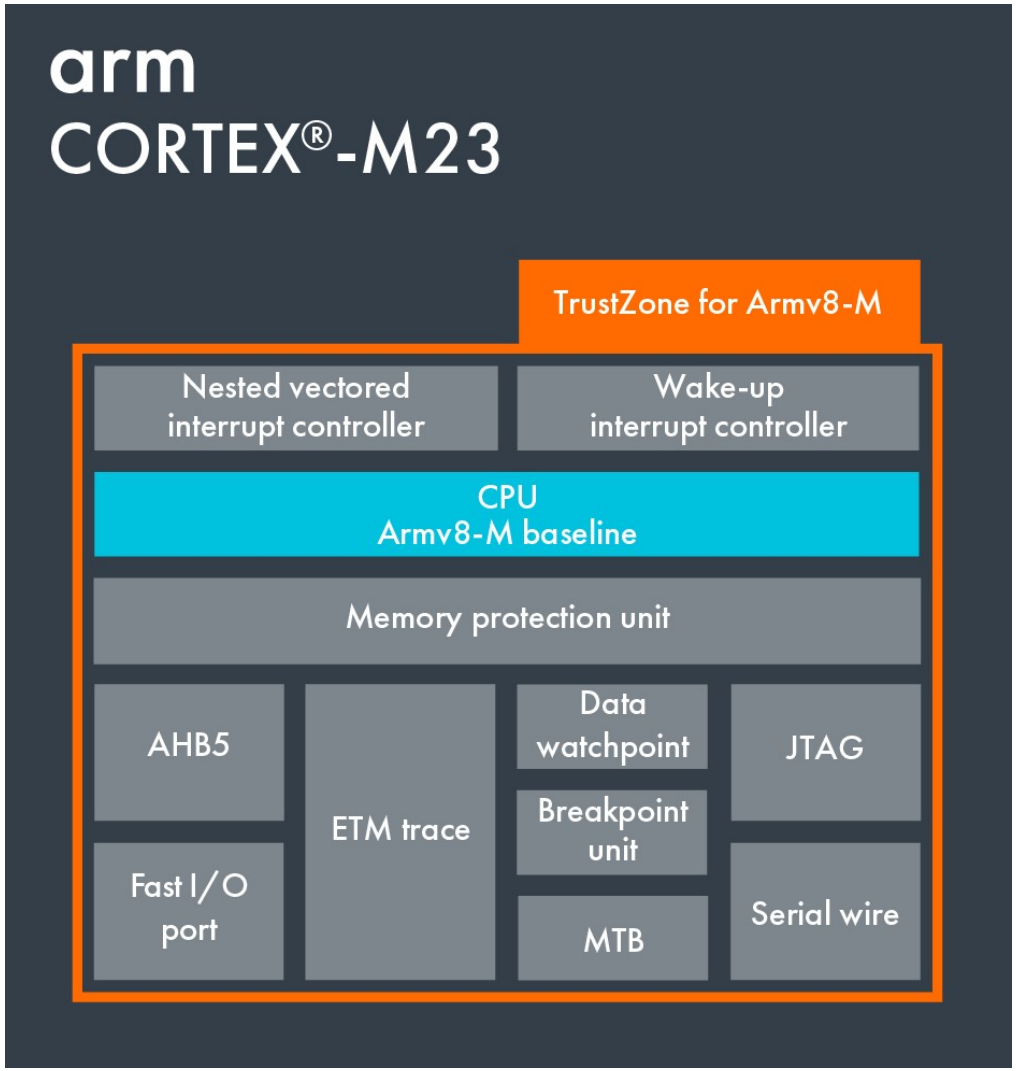


Trust Zone


Non-secure memory
Secure memory
Non-secure callable
Non-secure application
call
return
Secure entry point
call / branch
Secure library
return

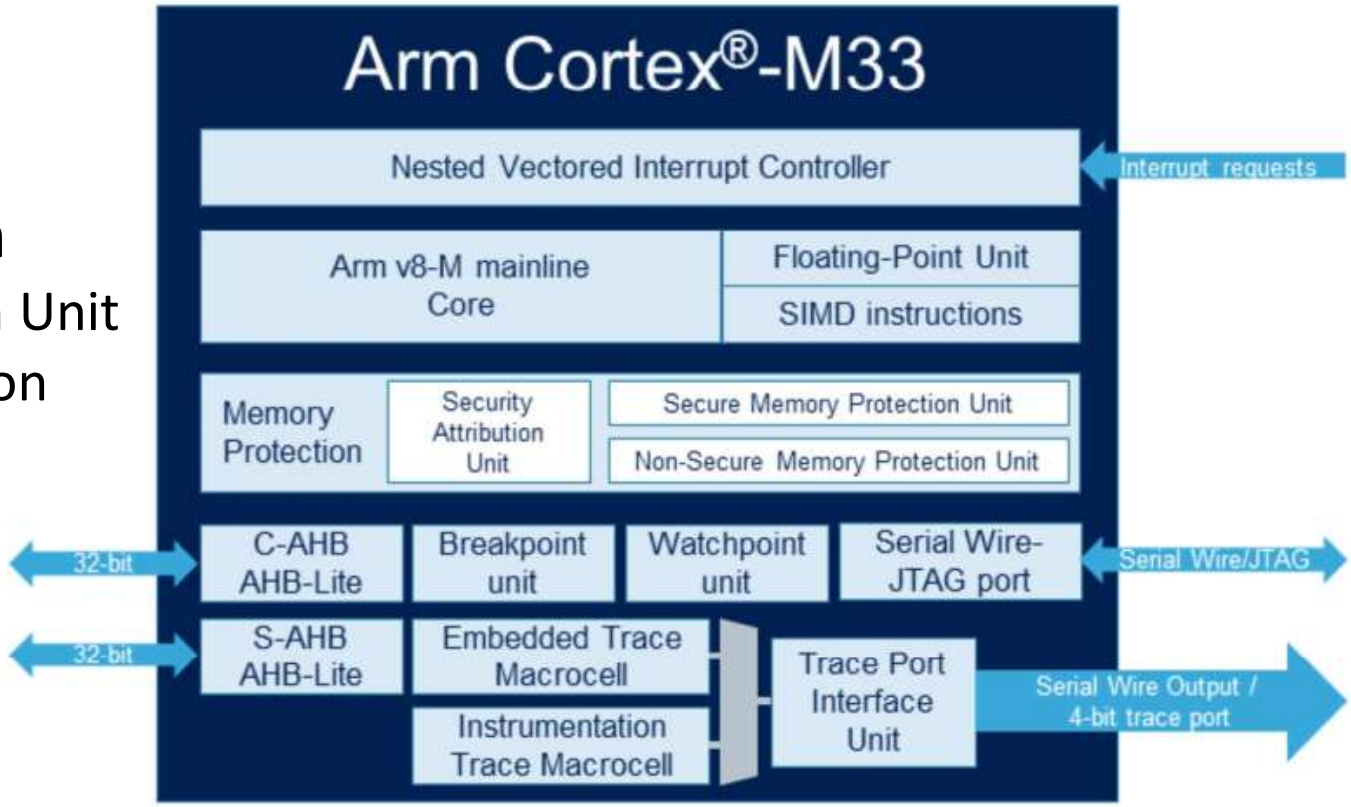
Cortex-M23

- ARMv8-M baseline architecture
- Stronger instructions than M0+
- 2 stage pipeline
- 0.98 DMIPS/MHz (M0+ 0.95)
- 2.64 CoreMark/MHz (M0+ 2.46)



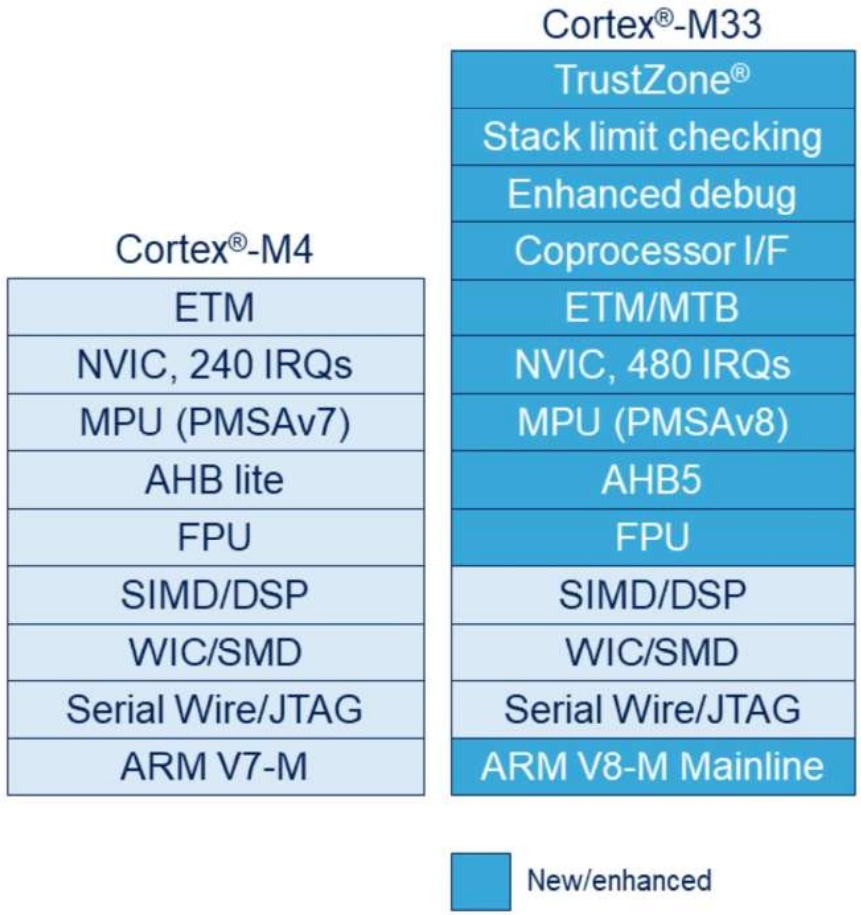
Cortex-M33

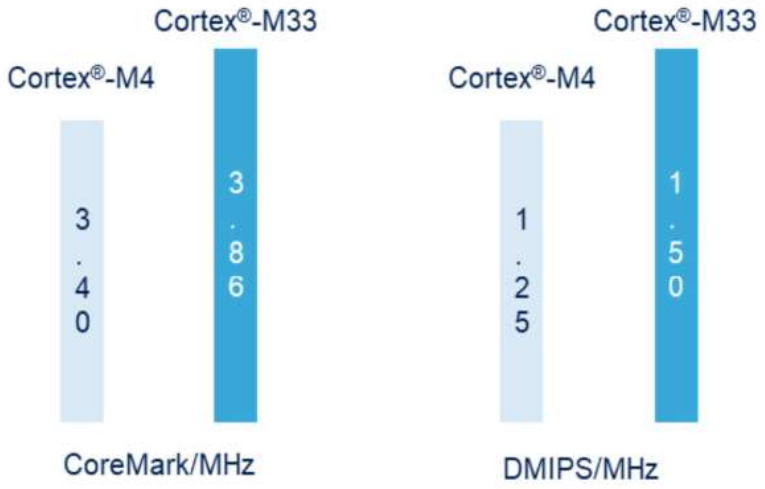
- ARMv8-M architecture
- Built in floating-point support
- SIMD instructions
- 3 stage pipeline
- Memory protection
  - Security Arbitration Unit
  - 2 Memory protection units



Cortex-M33 vs M4

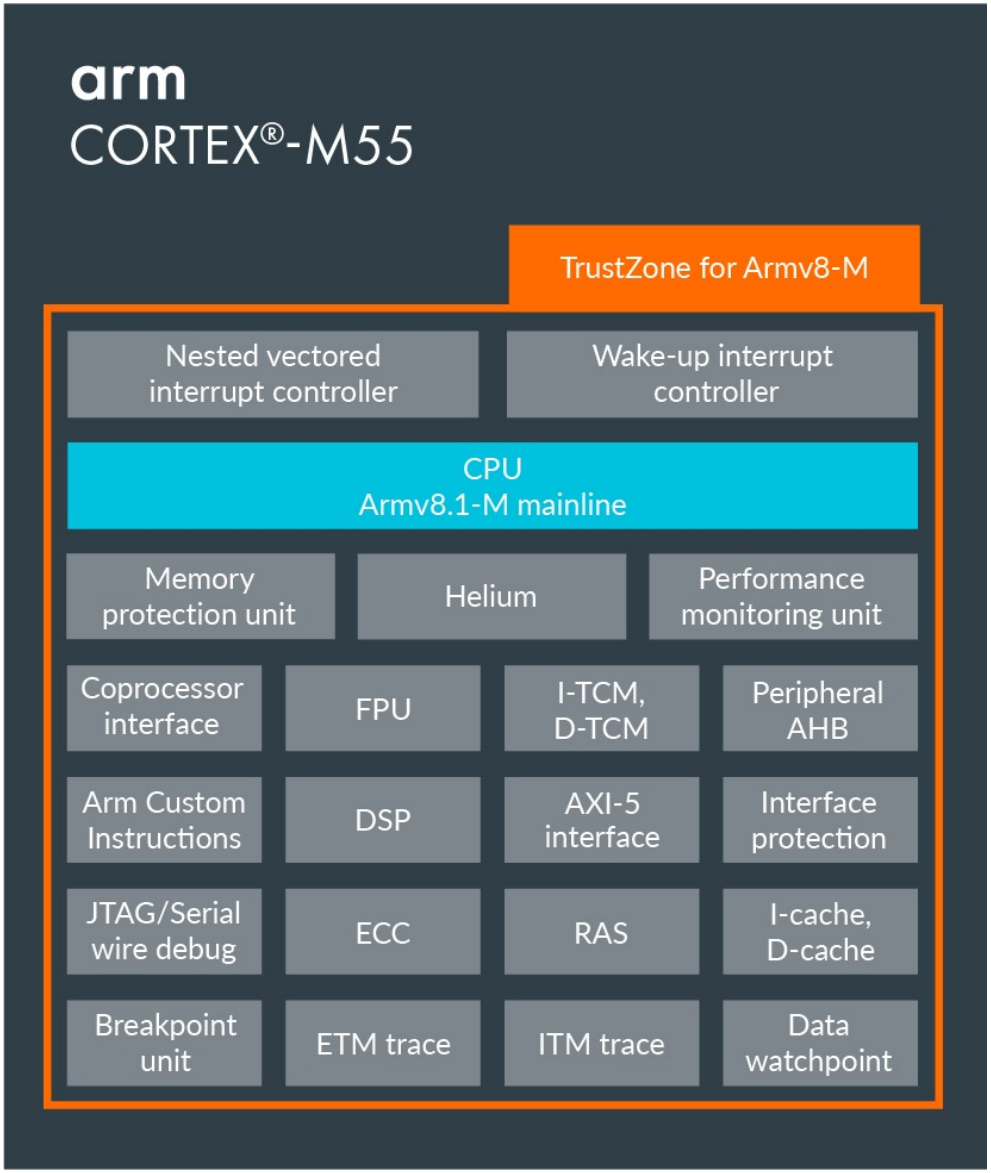
- Improved functionality
- Main difference is the TrustZone





Cortex-M55

- ARMv8.1-M mainline architecture
- 4 element pipeline
- Much more powerful floating point unit
- Helium extension for floating point vector operations
  - MI support
  - Edge support
- Instruction and data cache
- 1.6 DMIPS/MHz (1.25 DMIPS/MHz M4)



Cortex-M85

- ARMv8.1-M architecture
- 7-element pipeline
- 64-bit main bus system
- 32-bit SIMD instructions
- Helium extension for floating point vector operations
  - MI support
  - Edge support

- 3.13 DMIPS/MHz (2.14 M7)