ARM Cortex core microcontrollers

Requirements

Balázs Scherer

Méréstechnika és
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Tanszék

Homework

- Possibilities:
  - Usable hardware
    - Silabs: Energy Micro series, STM32F429i board, LPC 1768 mbed, Your preferred hardware
  - Topic
    - Individual or group
    - Your own topic, or a given one
- Conformance levels
  - OK: a low complexity homework to full fit the requirements
  - Good: More complex software, or some self-made hardware extension
  - Very good: Using high complexity software library-s like USB stack, or TCP/IP stack.
  - Outstanding: very high-level work

Homework: deadlines

- Selecting a topic
  - April
  - An email to me, with the sort description of the selected topic and used hardware
- Presentation of Homework
  - Last lecture
- Documentation of the homework
  - Documentation: Standard Technical Documentation 10 to 15 pages.

Resources, Exam

- Resources: Lecture ppt-s
- Exam
  - Given list of questions: ~40 questions
  - Exam: Randomly selected 10 question from the list
- Exam points:
  - Each question is 10 points: 100 points exam
  - Grade 1: 0 - 40 points
  - Grade 2: 41 - 55 points
  - Grade 3: 56 – 70 points
  - Grade 4: 71 – 85 points
  - Grade 5: 86 – 100 points
- Effect of the HW level
  - OK: 1 selected question is considered with maximum points.
  - Good: 2 selected questions …
  - Very Good: 3 selected question …
  - Outstanding: 4 selected question …

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1st Introduction: Brief history of microcontrollers

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The first microcontrollers (Intel MCS-48)

- 1976: Intel introduce a 8 bit microcontroller the MCS-48/49 (8048, 8049). In that year 251.000 pieces are sold from that series.
  - Internal 1-2k ROM, internal 64-256 bytes RAM
  - About 10 MHz clock speed
  - Many embedded control device and future PC peripheral used it.

Internal architecture of Intel MCS-48

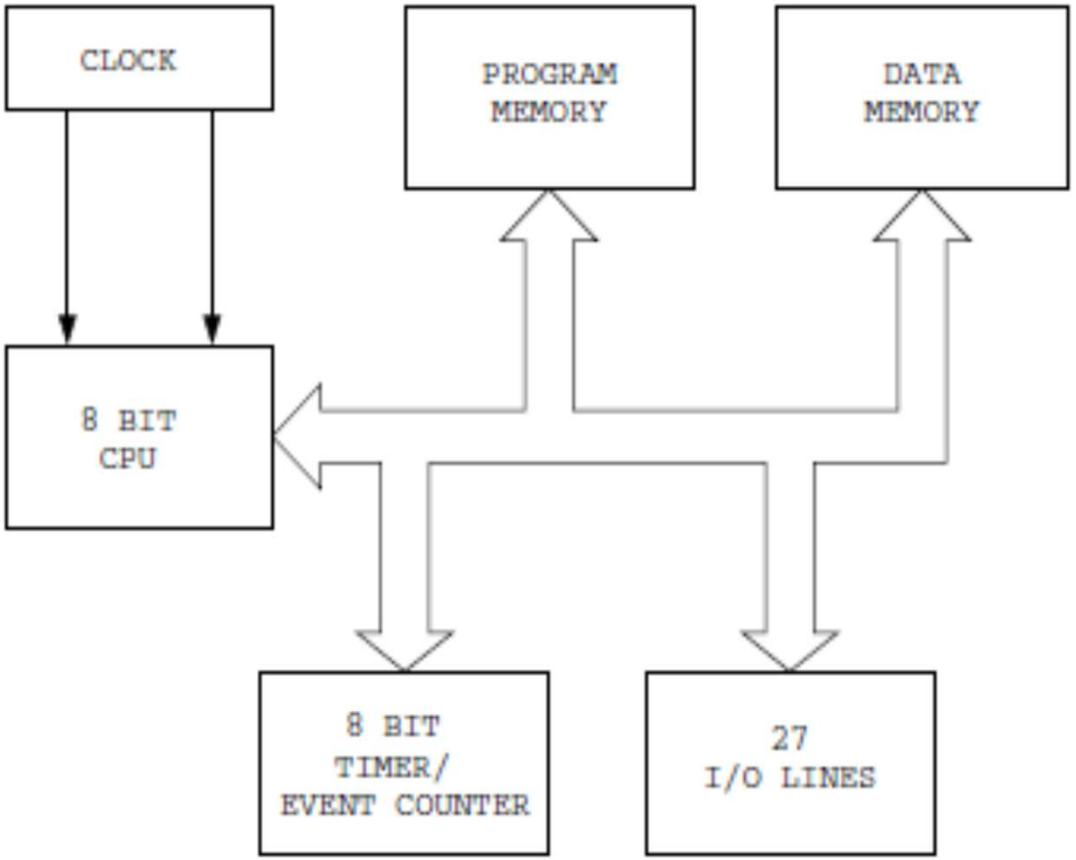


Figure 1.
Block Diagram

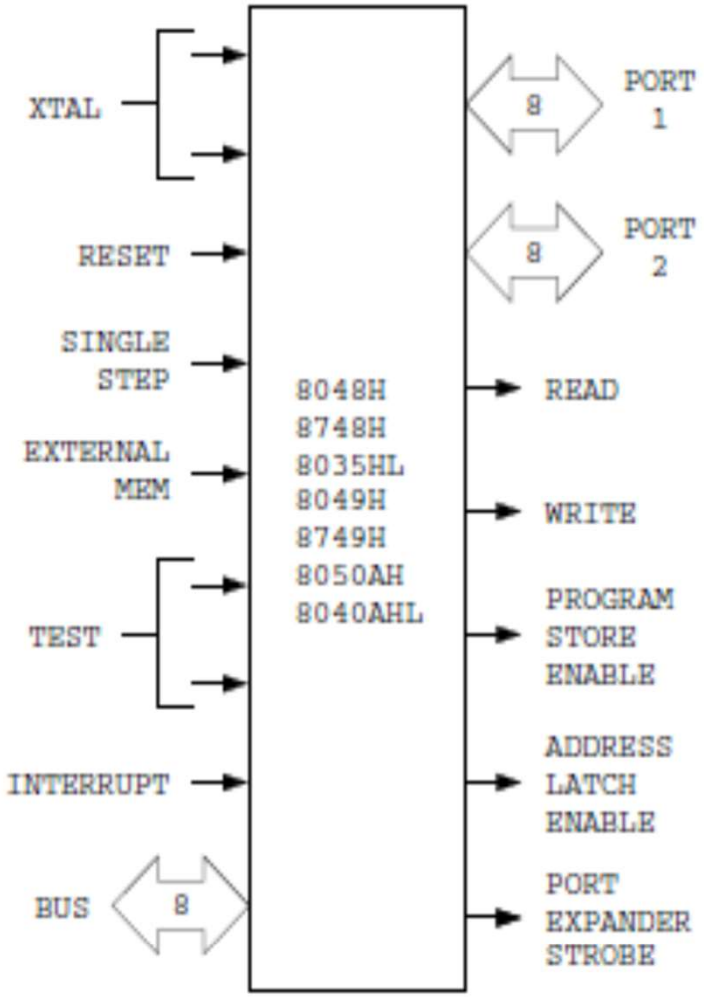


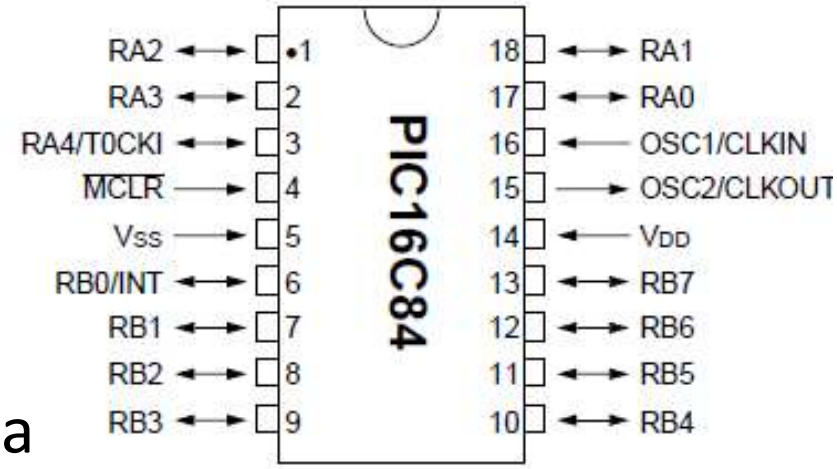
Figure 2.
Logic Symbol

Intel 8051

- 1980: Intel introduce the **8051** line. An 8 bit microcontroller with EPROM memory
  - https://www.youtube.com/watch?v=_sSuzDg4ntA
- 1983: 91 million of 8051 is sold
  - The most widespread line of the 80-s and 90-s
  - 8 bit ALU
  - 8 bit data bus
  - 16 bit address range: 64k RAM and ROM
  - On-chip RAM - 128 bytes
  - On-chip ROM - 4 kbytes
  - 4*8 bit bi-directional I/O port
  - UART
  - Two 16 bit Counter/timer
  - Power saving mode

1993: PIC 16C84

- **PIC**: Peripheral Interface Controller / Programmable Intelligent Computer
  - Originally designed by General Instruments to supports their 16 bit processor
  - In 1985 the General Instruments wind-up their uC design
  - Microchip redesign the line
- 1993 Microchip introduce the first PIC16C84 line microcontroller
  - **Novelty: EEPROM**.
  - Development is cheaper and faster
  - Small companies can use it
  - EEPROM program memory: 1k
  - EEPROM 64 byte, 36 byte SRAM data



1997: Atmel ISP Flash based micro

- 1993 Atmel introduce the first Flash based microcontroller
  - Based on the 8051 core
  - Needs a Flash burner to program it
- 1997 Atmel introducing the their own AVR core microcontroller
  - In-System programable: there is no need for a separate flash burner
  - AT90S8515
    - 8 kByte Flash
    - 512 Byte SRAM
    - 512 Byte EEPROM
    - UART
    - SPI
    - PWM
    - 32 I/O line

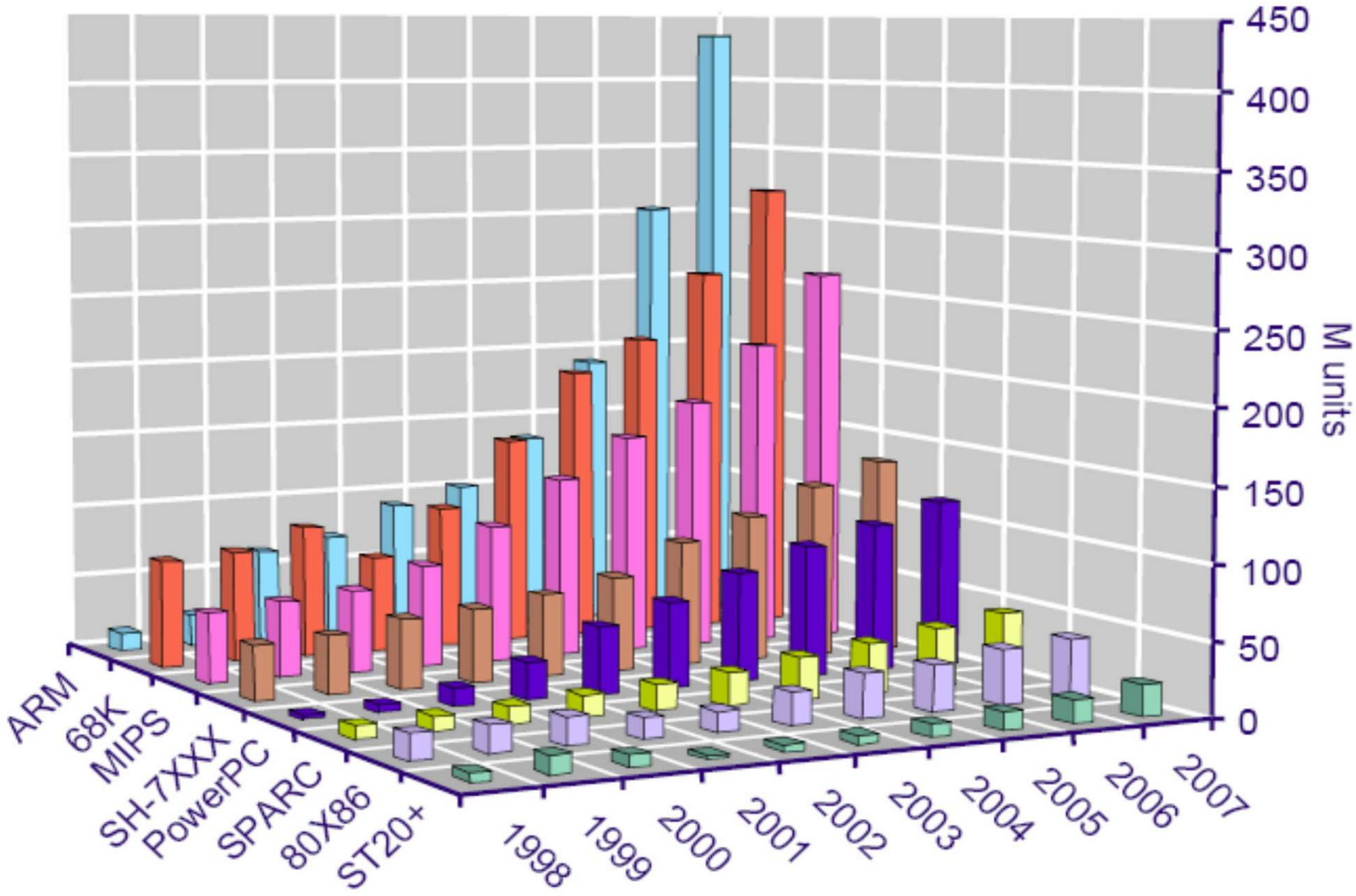
2003: Philips (NXP) LCP210x line

- 2003 Philips introduce the first 32 bit ARM 7 core microcontroller with in chip program and data memoryNXP:
  - LPC2104,LPC2105, LPC2106
- All the other manufacturers introduce their ARM 7 core micro
  - NXP: LPC2xxx line
  - Atmel: AT91SAM7
  - Texas Instruments: TMS470
  - Analog Devices: ADuC70xx
  - STMicroelectonics: STM7
- 2005 Introduction of the first ARM9 micro

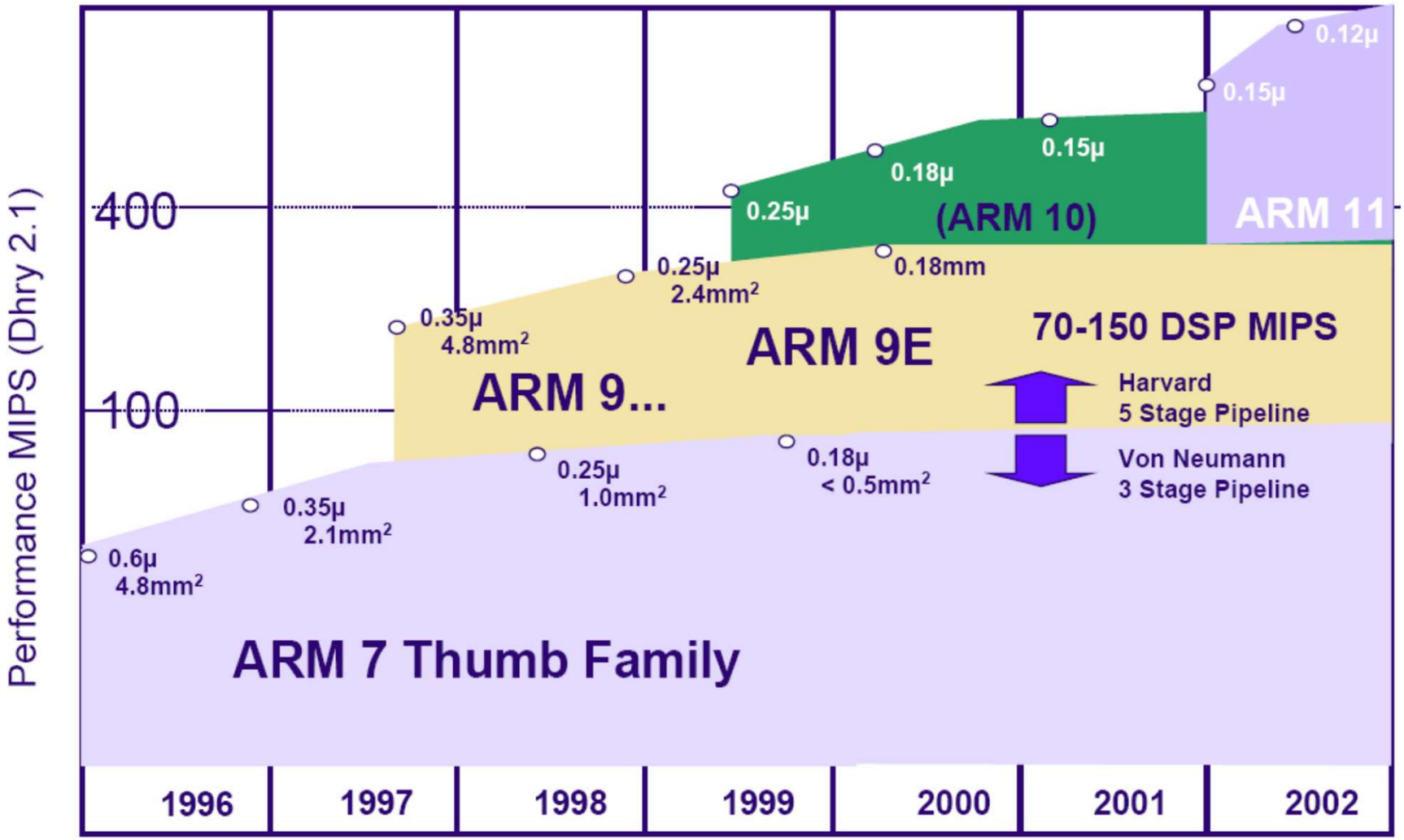
Why ARM?

- ARM is founded in 1990 as a joint venture by Acorn Computers, Apple Computer and VLSI Technology
- Az Advanced RISC Machines Ltd (ARM) design IPs, mainly processor cores. There is no such as ARM microcontroller.
- Many microcontroller or chip manufacturers uses the ARM cores and ARM IPs (NXP, ST, Texas, Atmel, OKI, Samsung, Sony stb.).
- The most known processor core provider.

Comparing ARM to other architectures (2007)

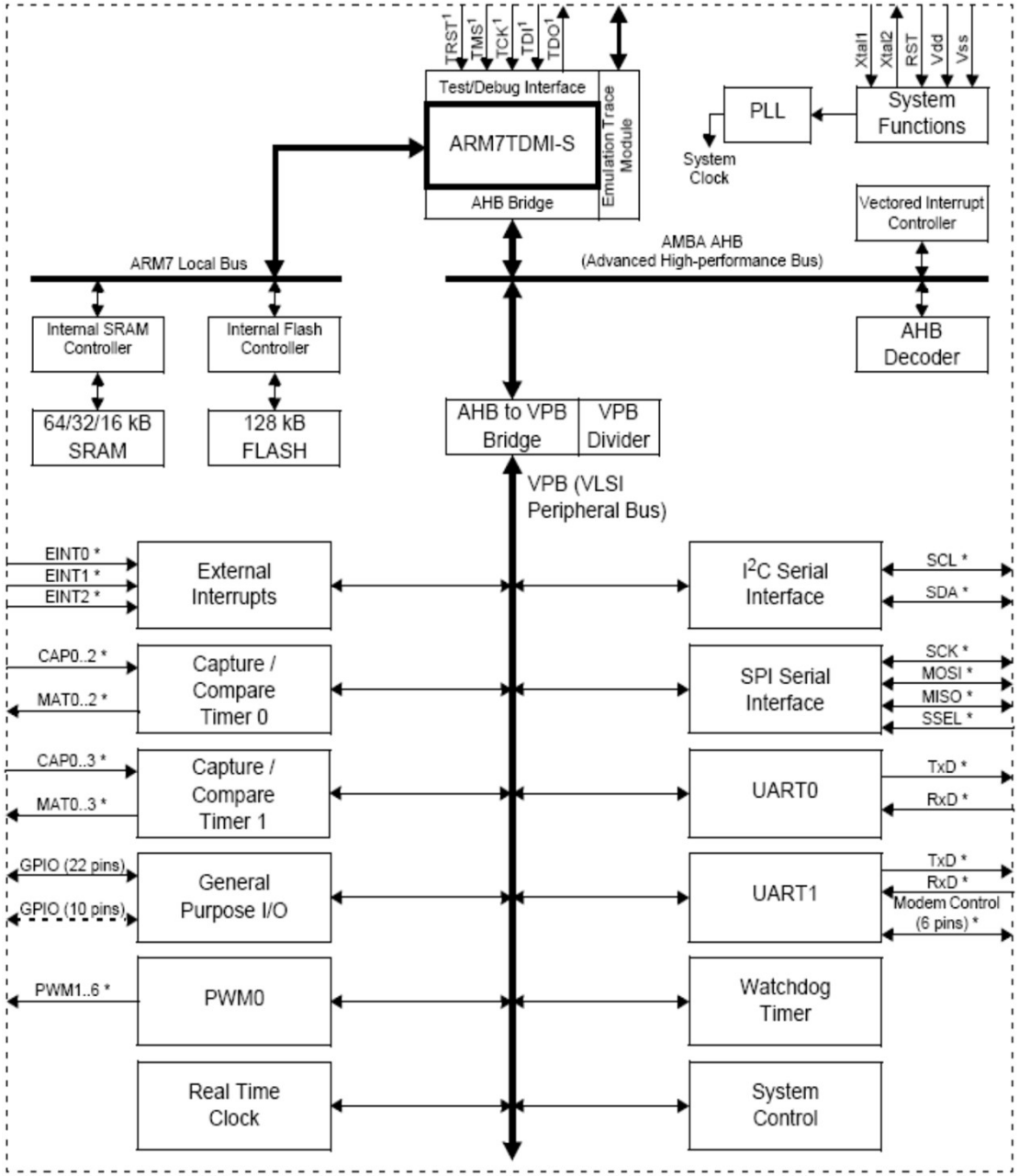


Traditional ARM cores



2003: LPC2106

- 128 kByte Flash
- 64 kSRAM
- 60 MHz
- 2 SPI
- UART
- I2C

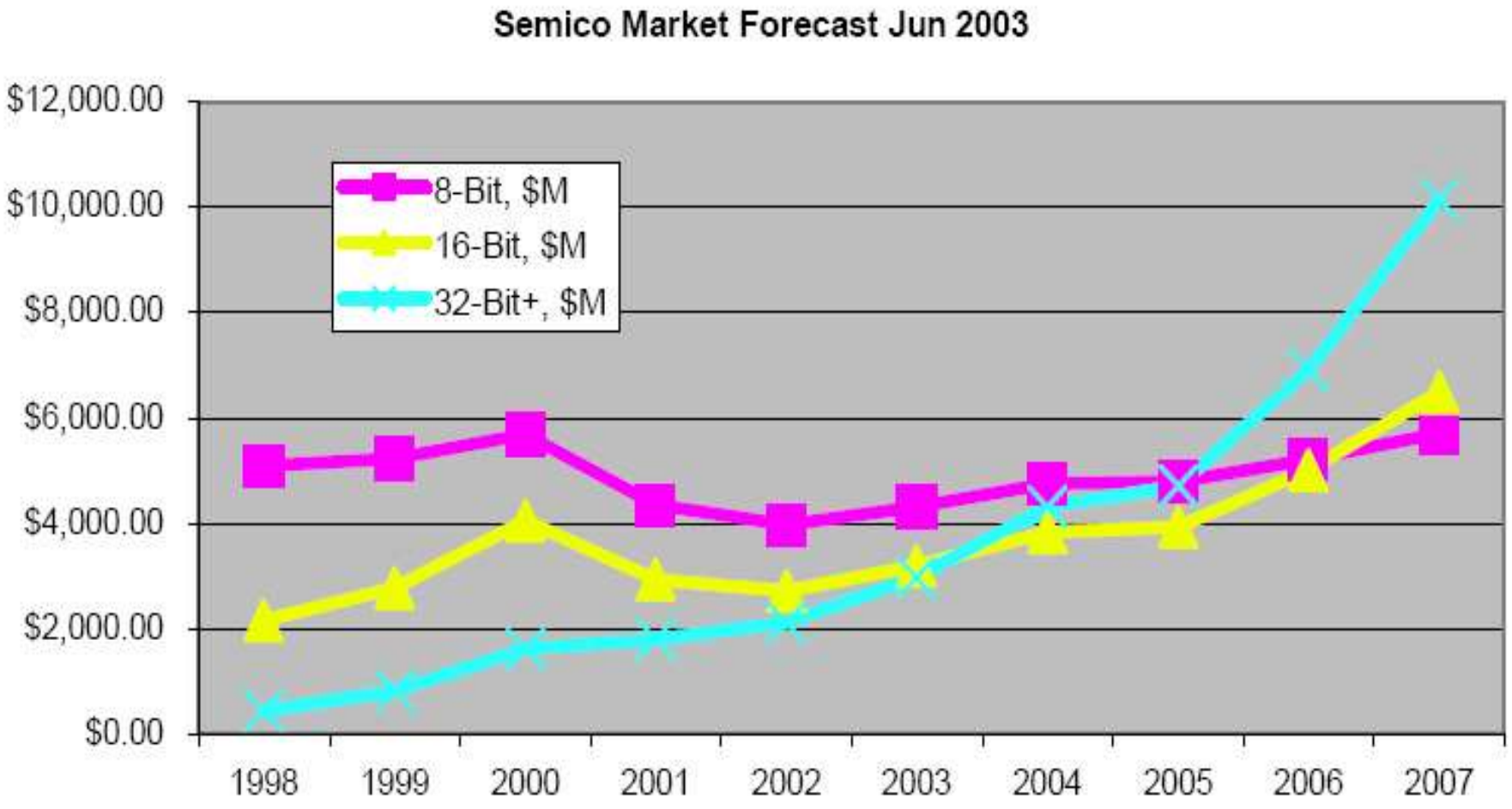


Snapshot of the microcontroller market in 2003

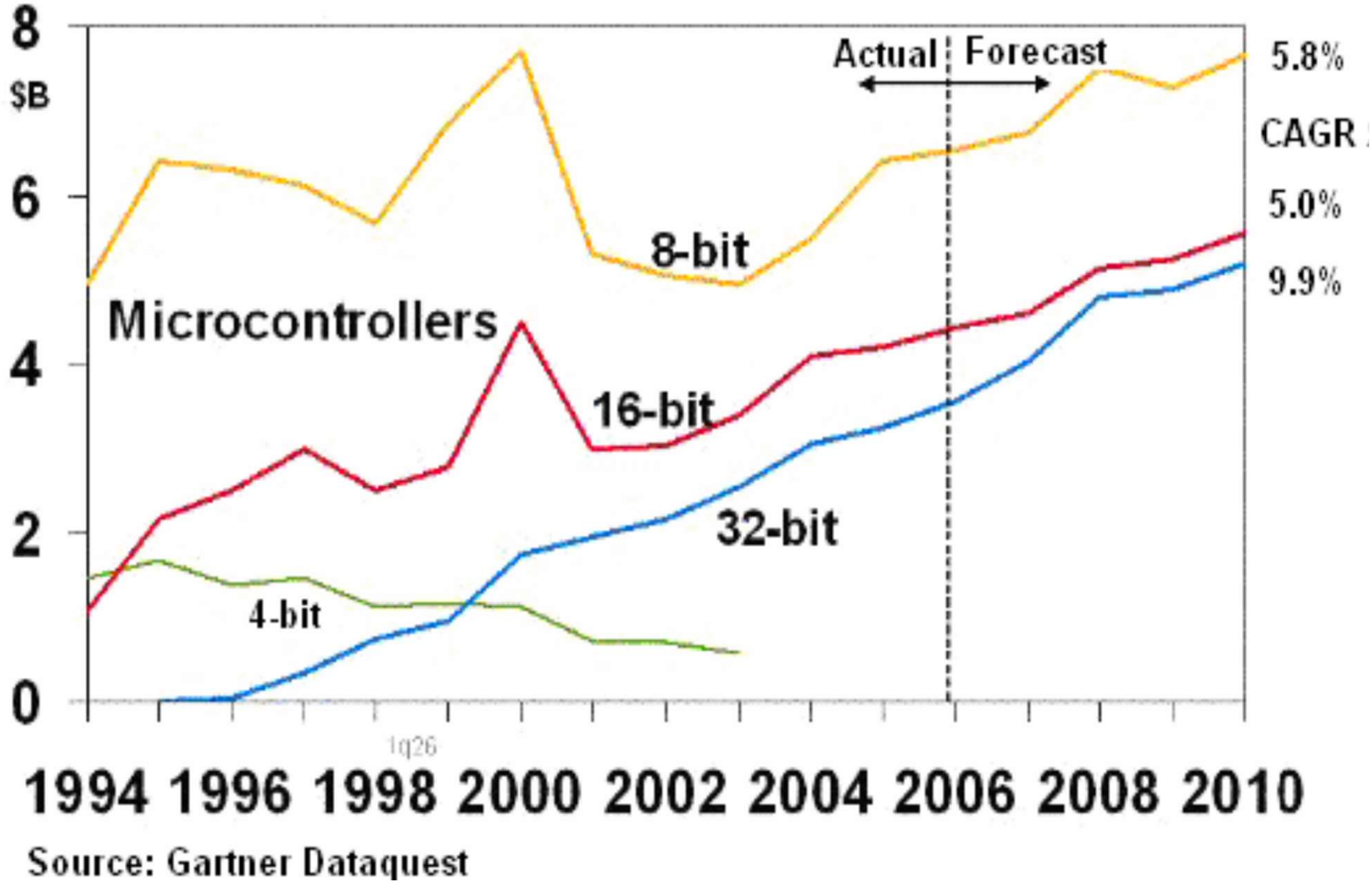
Microcontroller	PIC18F452PIC	ATmega128AVR	LPC2106ARM
Flash/ SRAM/ EEPROM	32k / 1,5k / 256	128k / 4k / 4k	128k / 64k
MIPS	10	16	50
Data bus	8	8	32
GPIO	36	53	32
ADC	10bit 8channel	10bit 8channel	0
Peripherals	SPI, I2C, UART, 4 Timer	SPI, I2C, UART, 2 8bit Timer, 2 16bit Timer	SPI, 2UART, I2C, 2 32bit Timer
Power consumption	15-25mA (4.2V) ~105mW	25-30mA (4.5V) ~135mW	40-50mA (3.3/1.8V) ~125mW
Price (for 100 pieces)	$6.51	$8.81	$9.48

Market prognosis in 2003

Figure 1. Semico microcontroller market forecast, June 2003



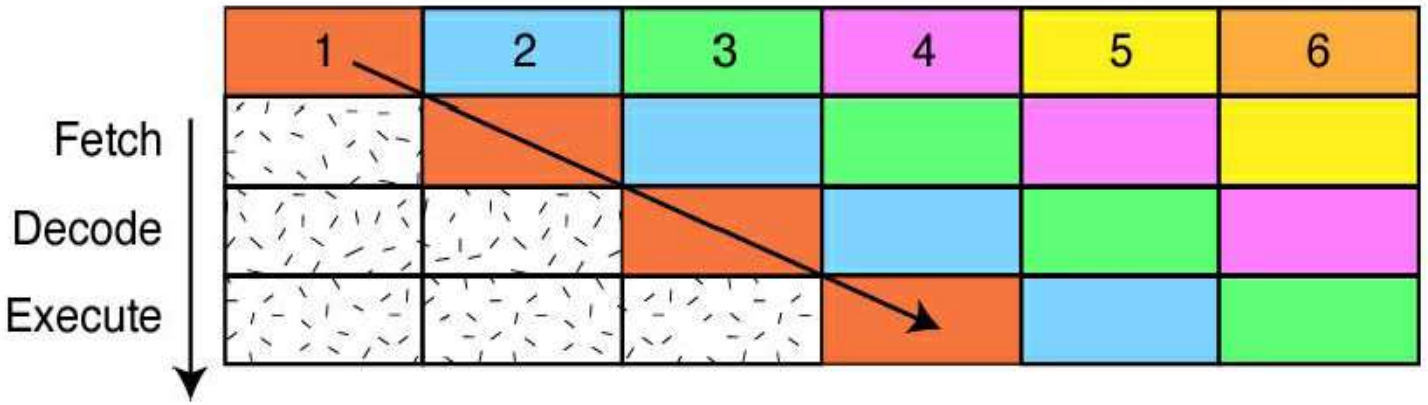
Market prognosis in 2006



The ARM 7 core

The ARM 7 core (ARMv4)

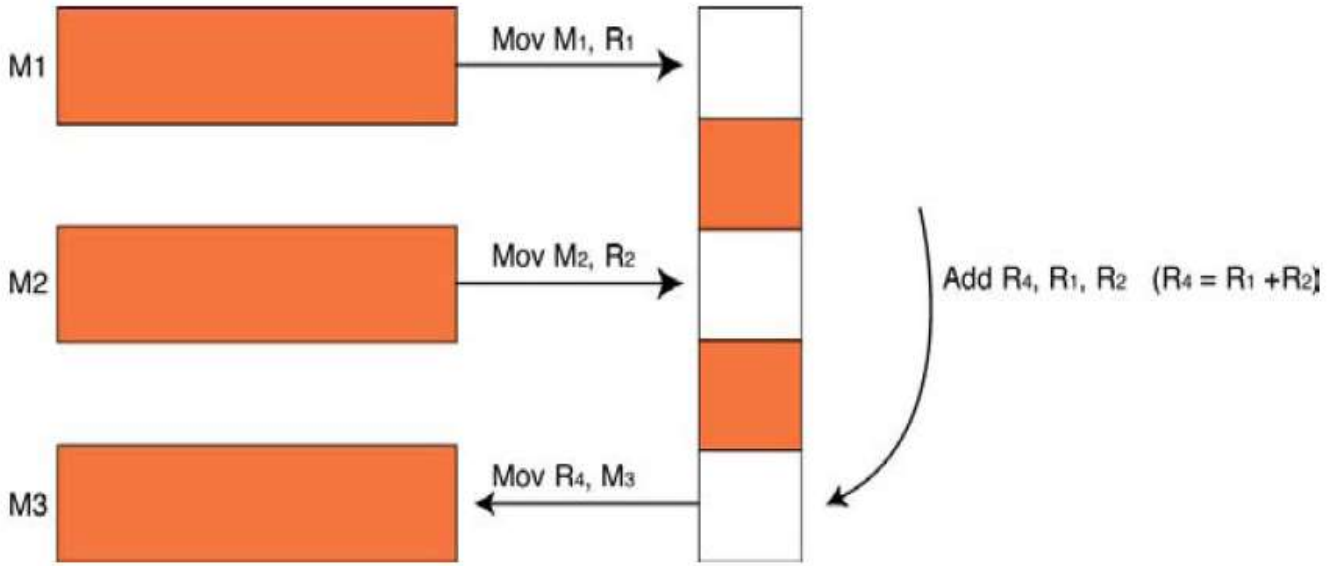
- Reduced instruction set, small complexity
  - Fast, and power efficient
- Pipeline based instruction execution
  - 3 stage pipeline
  - Most instruction has 1 clock edge execution



The ARM7 three-stage pipeline has independent fetch, decode and execute stages

Load and Store architecture

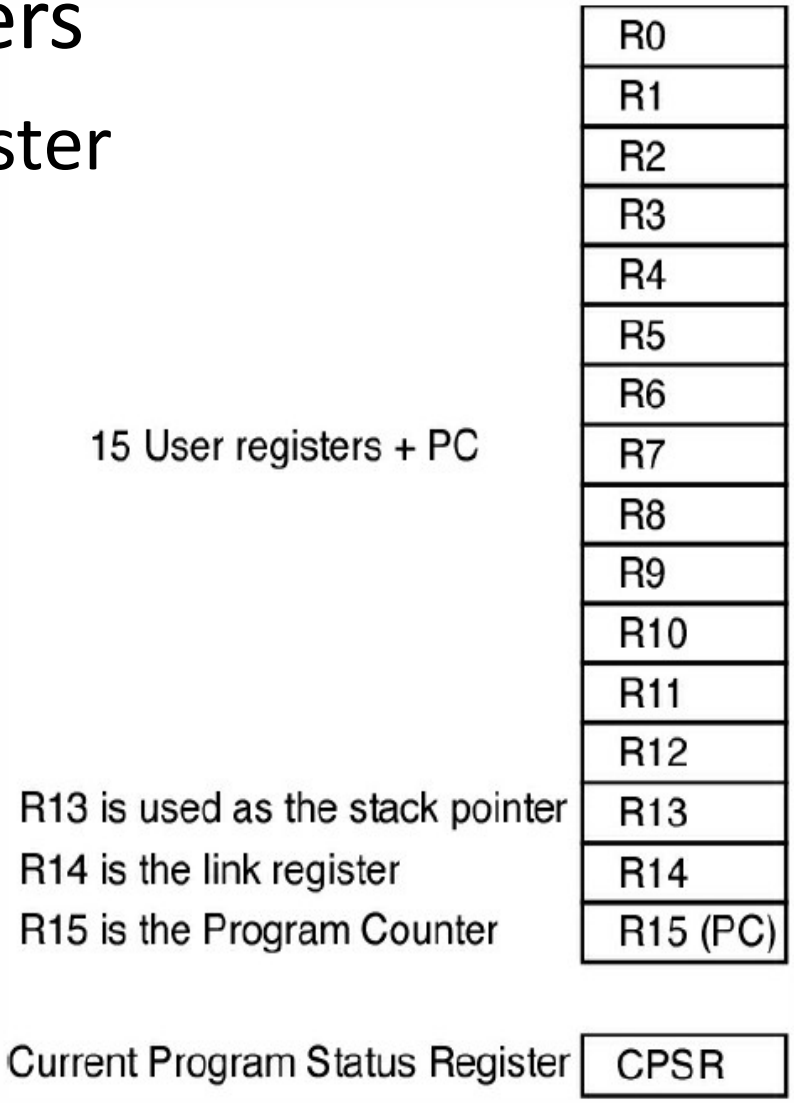
- First the data needs to be loaded from the memory to a register, then the operation can be executed using the data in the registers, then the result is written back to the memory



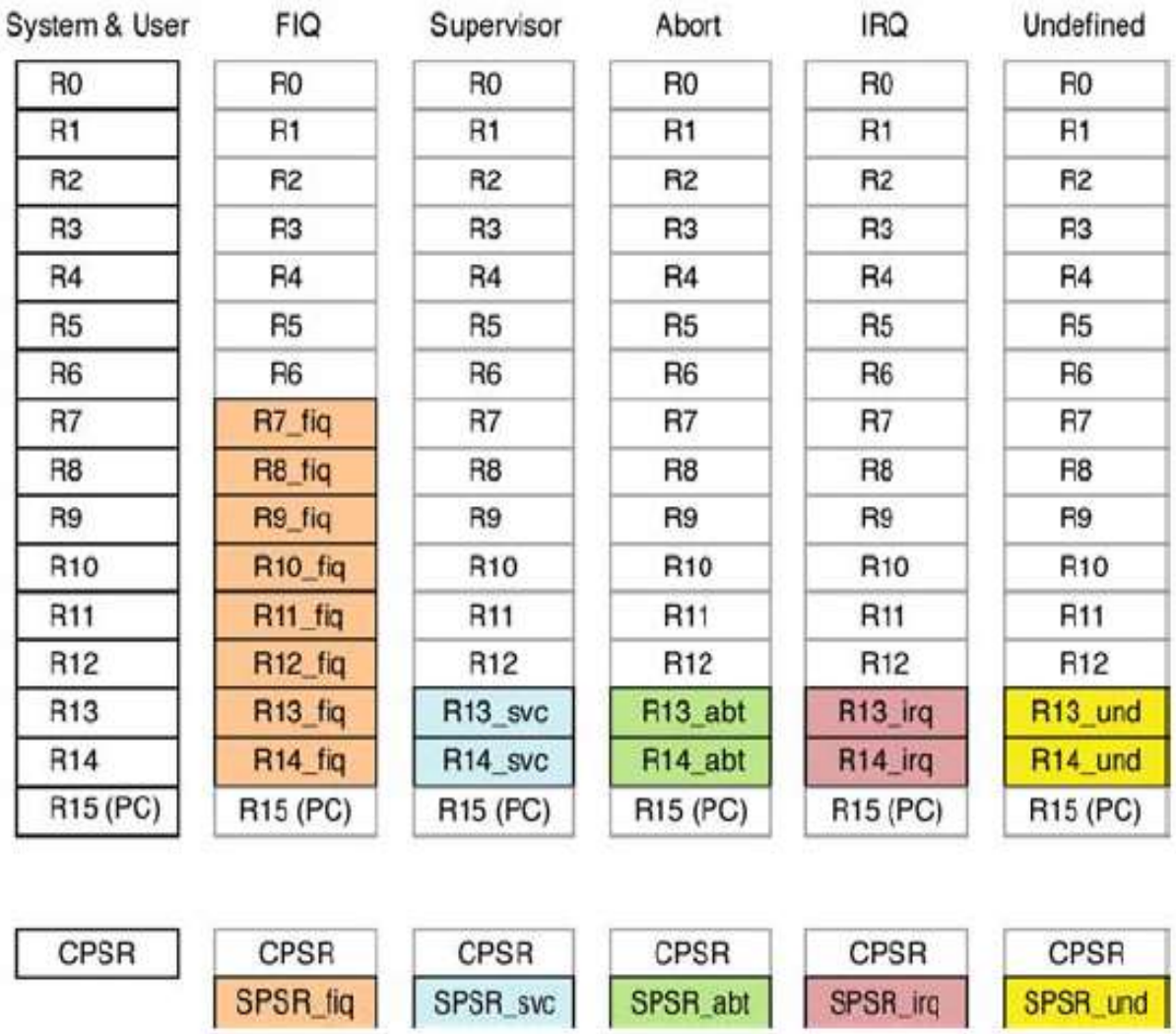
The ARM7 CPU is a load-and-store architecture. All data processing instructions may only be carried out on a central register file

Register set

- General purpose registers
  - 16 general purpose register
  - CPSR
    - Operating mode
    - IT enable
    - Thumb/ARM
    - Conditions
      - Zero
      - Negativ
      - Carry
      - Overflow



Operating modes



The ARM7 CPU has six operating modes which are used to process exceptions. The shaded registers are banked memory that is "switched in" when the operating mode changes. The SPSR register is used to save a copy of the CPSR when the switch occurs

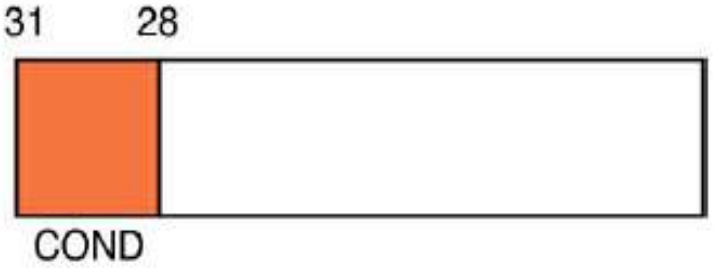
Event handling

- Very basic event handling
  - Vector interrupt controllers were provided by the microcontrollers manufacturers
  - Not efficient, and hard to port the code from one uC to another

Exception	Mode	Address
Reset	Supervisor	0x00000000
Undefined instruction	Undefined	0x00000004
Software interrupt (SWI)	Supervisor	0x00000008
Prefetch Abort (instruction fetch memory abort)	Abort	0x0000000C
Data Abort (data access memory abort)	Abort	0x00000010
IRQ (interrupt)	IRQ	0x00000018
FIQ (fast interrupt)	FIQ	0x0000001C

ARM instructionset

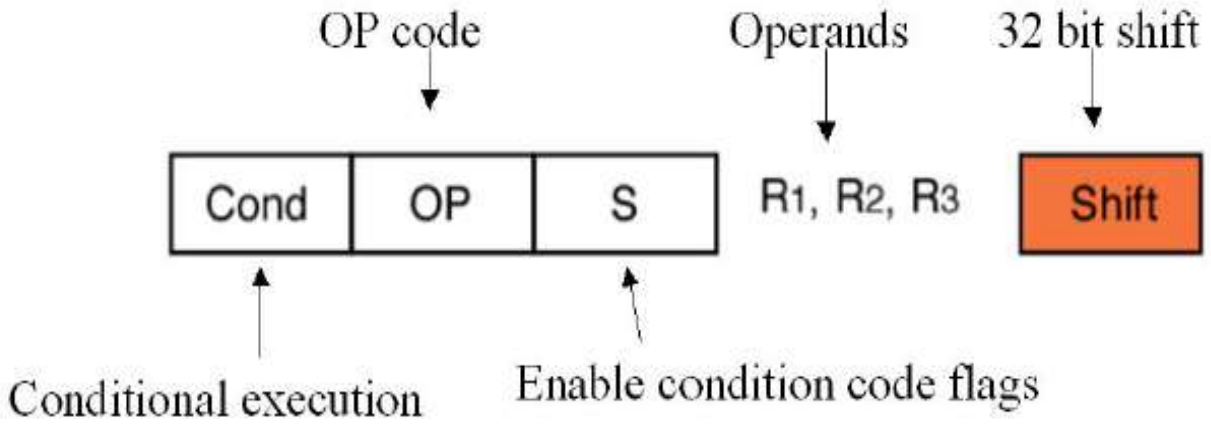
- Little-endian/Big-endian: hard wired configuration (microcontrollers are usually Little-endians)
- 32 bits ARM,16 bits THUMB instruction set (Thumb is 30% smaller, but 40% slower)
- Every arithmetic instruction is conditionally executed.
- Make the assembly coding a nightmare
- Help feeding the pipeline and enables a fast instruction execution



Every ARM (32 bit) instruction is conditionally executed. The top four bits are ANDed with the CPSR condition codes. If they do not match the instruction is executed as a NOP

Data processing ARM instructions

- Data processing
  - Using registers as operands
  - AND, OR, XOR, ADD, SUB, CMP…
  - If (z==1) R1 = R2+(R3x4)
  - EQADDS R1,R2,R3,LSR #2



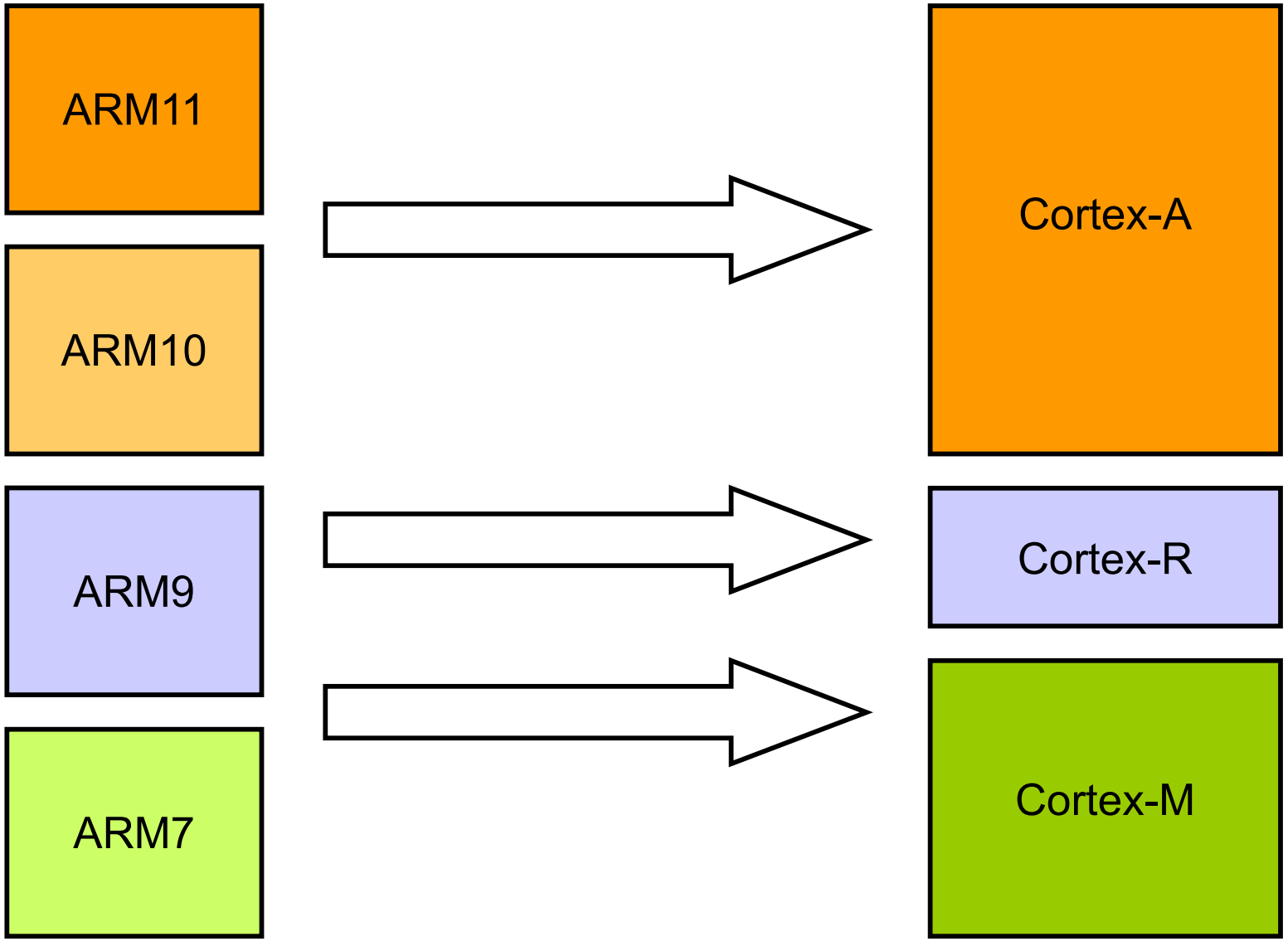
The general structure of the data processing instructions allows for conditional execution, a logical shift of up to 32 bits and the data operation all in the one cycle

ARM instruction and compilers

Parameter	Compiler			
	Keil CA BETA	GNU V3.22	ARM ADS V1.2	IAR V4.11A
Execution Speed (µSeconds)	25.4	112.9	16.8	24.4
Dhrystones/sec	39,370.1	8,857.4	59,382.4	40,983.6
Total Code Size (bytes)	10,330	36,004	22,266	19,892
Stack Size (bytes)	208	852	608	356
Total Data Size (bytes)	10,256	11,912	10,256	10,269

All tests were performed under identical conditions using the Keil µVision Simulator. The ARM device used was a Philips LPC2294 running at 60MHz in Thumb Mode.

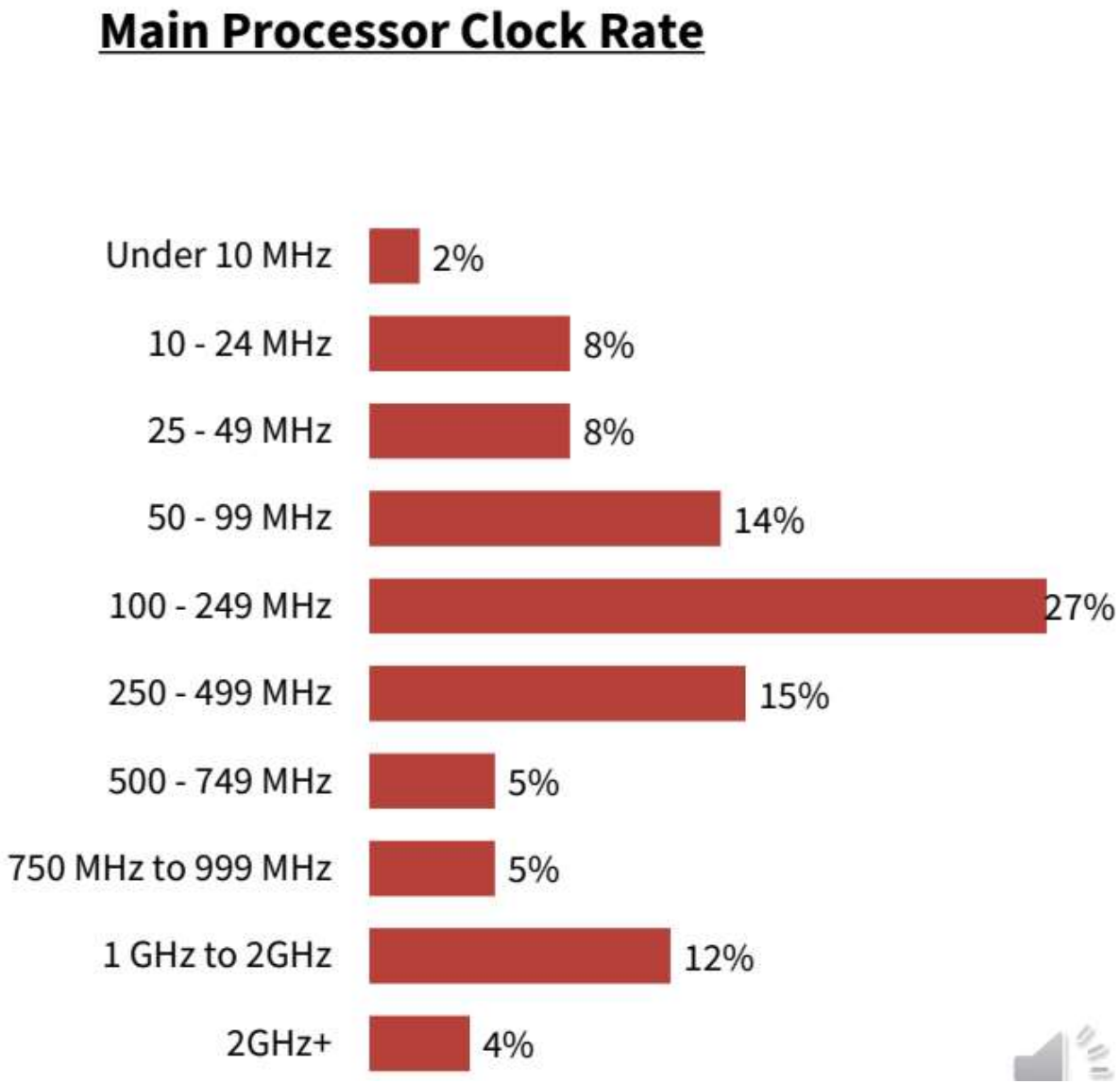
New generation of ARM cores



ARM Cortex

- Cortex-M3, the first line, introduced in 2006
  - Luminary Micro: Stellaris, STMicroelectronics: STM32F1xx, NXP: LPC17xx
- Cortex-M0, M0+ introduced in 2009
  - NXP, LPC11xx
  - STMicro: STM32F0xx
- Cortex-M4 introduced in 2010
  - NXP, LPC4xxx
  - STMicro: STM32F4xx
- Cortex-M7 introduced in 2015
  - STMicro: STM32F7xx
- Cortex-M33, Cortex-M23 first micros: 2019
  - ST STM32 L5, Nordic nRF91.
- Cortex-M85 fist micros: 2022

Clock speed of currently used processors (2023)



Current 32-bit processors (2023)