Development processes, lifecycle, V-model

VIMIMA11 Design and integration of embedded systems

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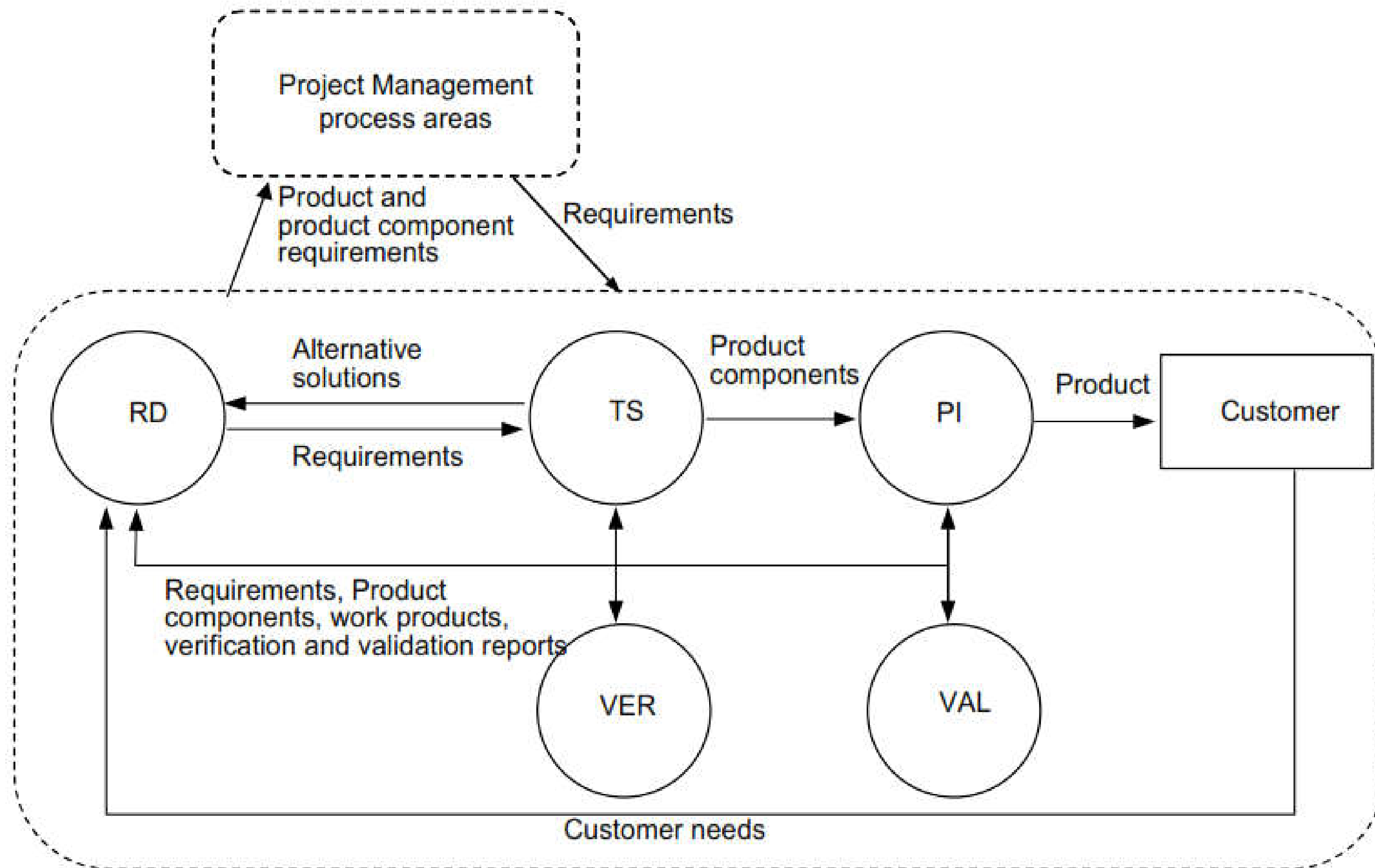
Lifecycle of a development process

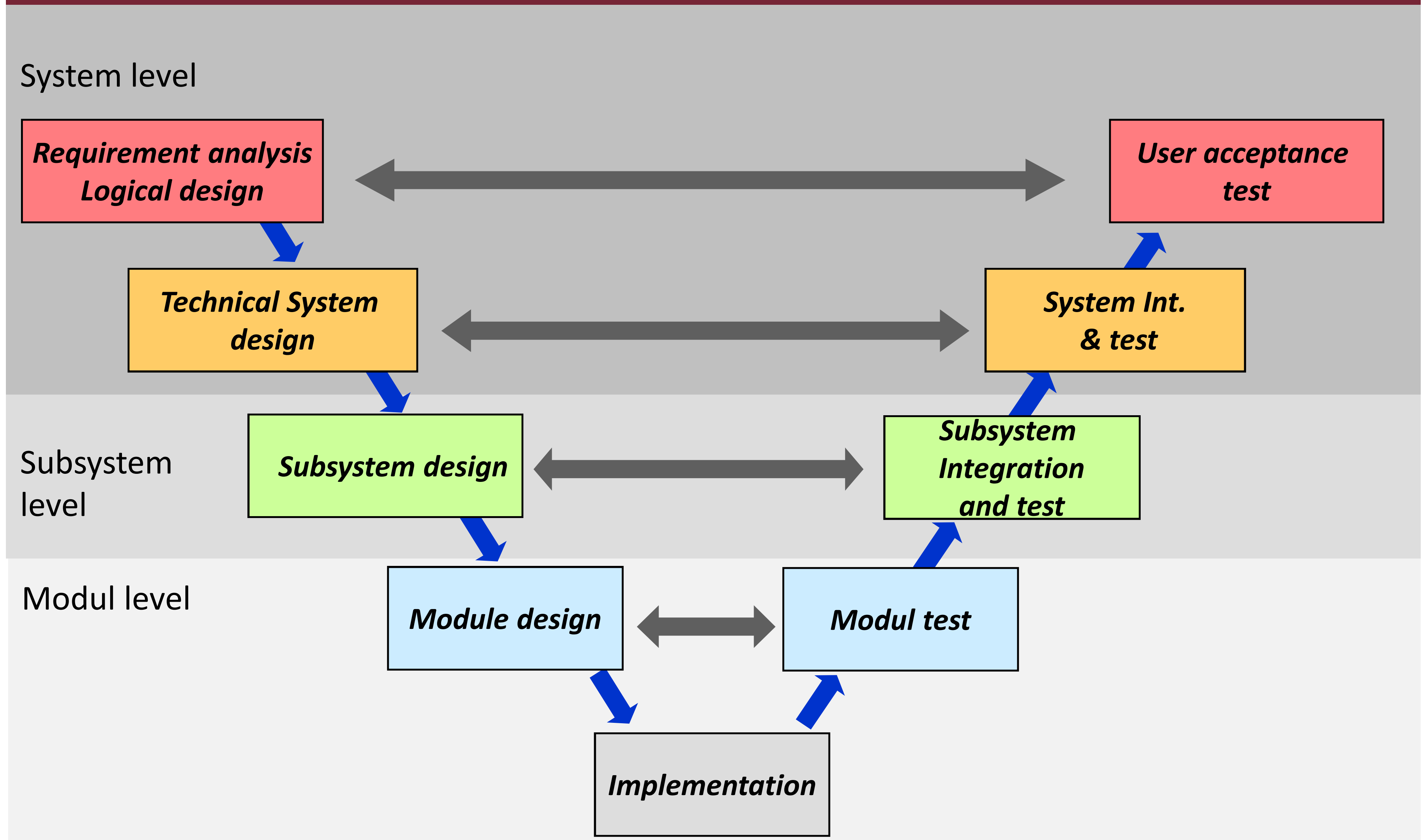
CMMI process areas connected to development life cycle



Development life cycle processes

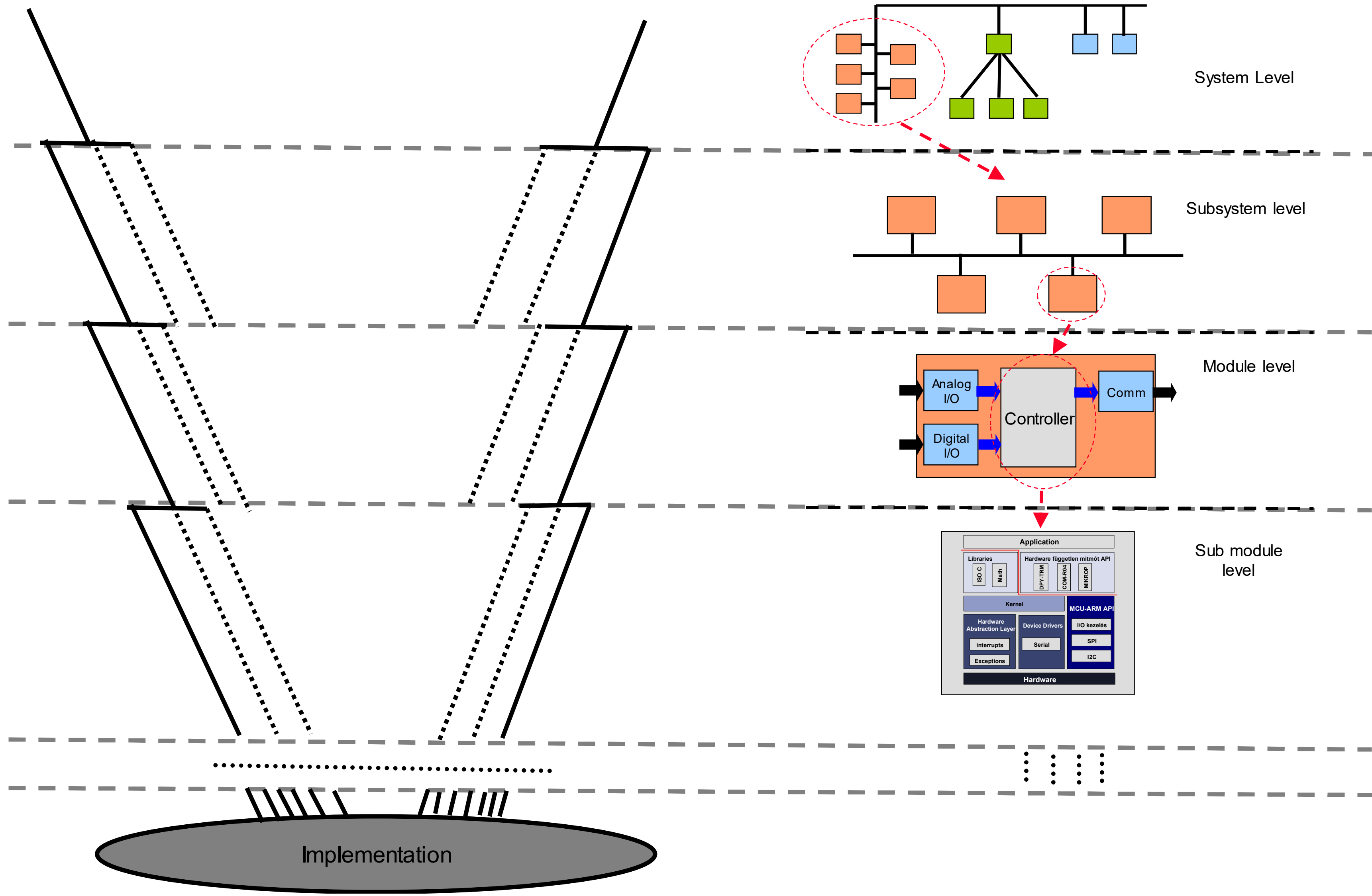
- CMMI describes the objectives and activities to be performed, but it do not specify a lifecycle
- Most of the companies are using existing lifecycle models for this purpose
  - Waterfall
  - Spiral
  - V-model

The V-model

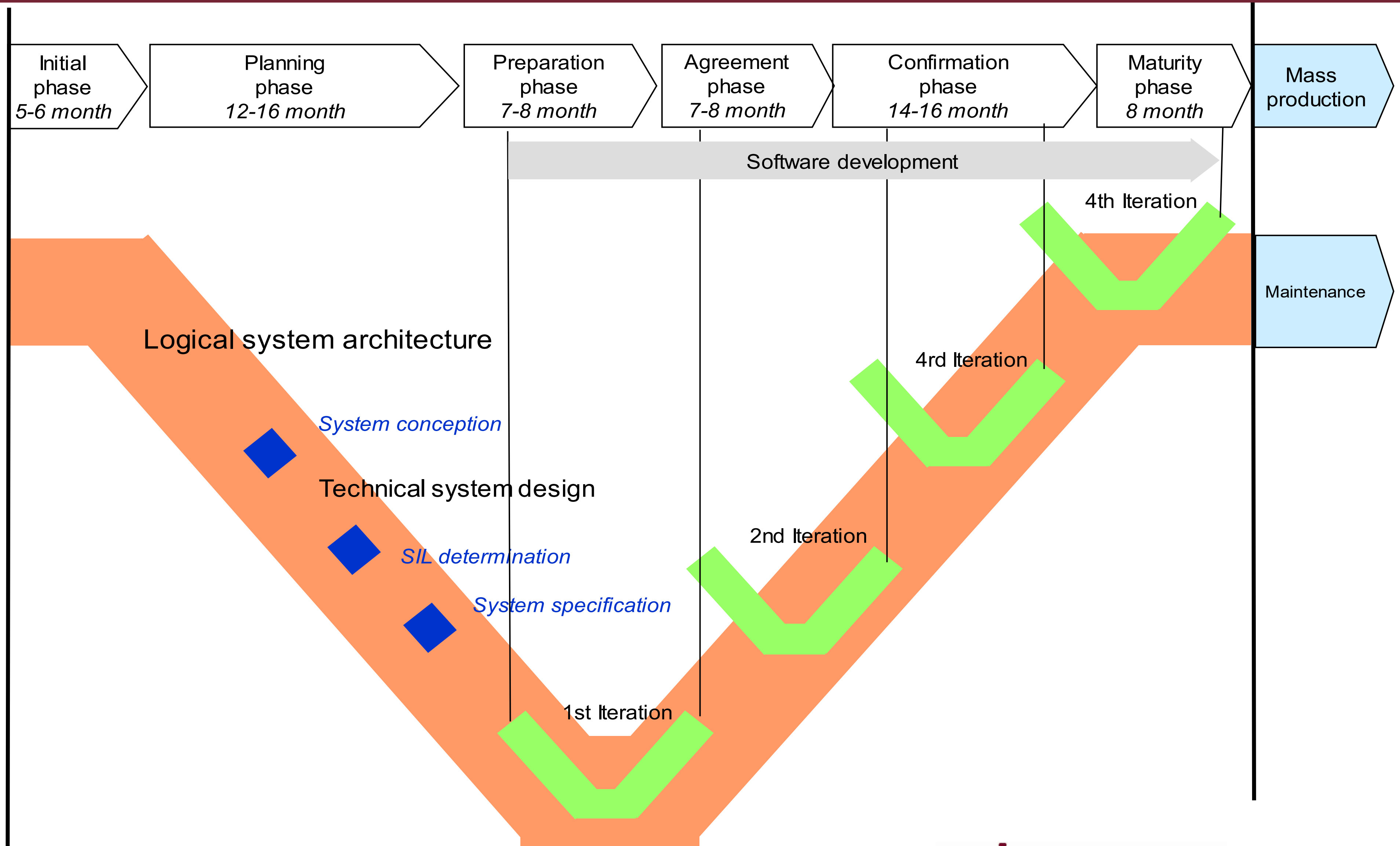


The V-model in the real world

V-model in real world

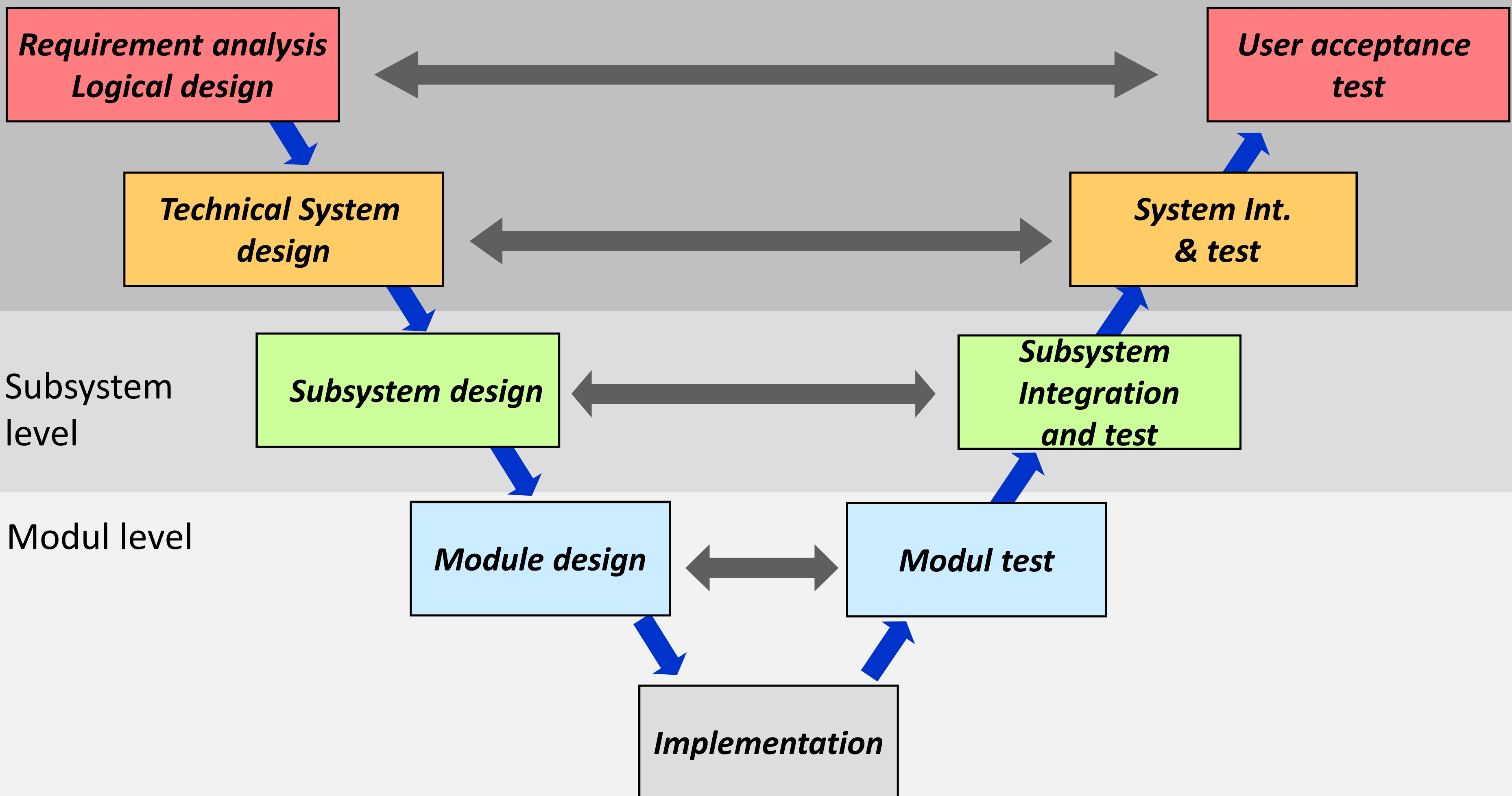


V-model in real world

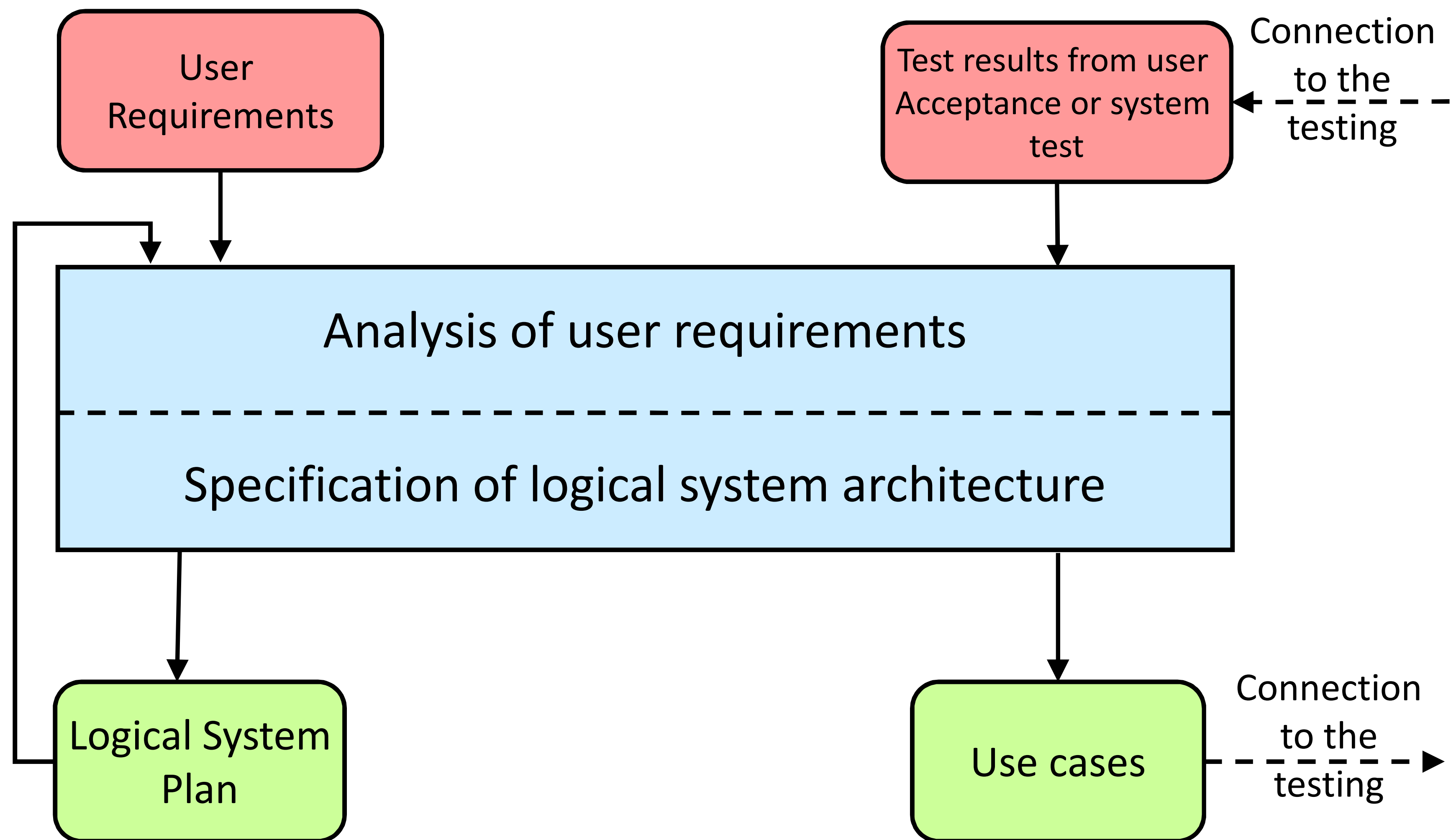


The steps of the V-model

Analysis of user requirements, designing the logical system architecture



Analysis of user requirements, designing the logical system architecture



CMMI process areas of requirement handling

Requirements development

- **SG 1: Develop Customer Requirements**
  - **SP 1.1:** Elicit Needs
    - Brainstorming, surveyment, prototype building, demonstrations, User Stories.
  - **SP 1.2:** Transform Stakeholder Needs into Customer Requirements
    - Translate stakeholder needs, expectations, constraints, and interfaces into documented customer requirements.
    - Establish and maintain a prioritization of customer functional and quality attribute requirements.
    - Define constraints for verification and validation.

Requirements development

- **SG 2: Develop Product Requirements**
  - **SP 2.1:** Establish Product and Product Component Requirements

    Transforming the user requirements into technical form, and explicit values.

    Example A carryable device: weight <2 kg, Size < 20x30cm, Battery system: voltage of the battey, capacity for 3 days

    Reliable: availability 99%

    Example: **House of Quality Function Deployment**
    http://www.webducate.net/qfd/qfd.html
    https://www.youtube.com/watch?v=u9bvzE5Qhjk

  - **SP 2.2:** Allocate Product Component Requirements
  - **SP 2.3: I**dentify internal and external Interface Requirements

Requirements development

- **SG 3: Analyze and Validate Requirements**
  - **SP 3.1:** Establish Operational Concepts and Scenarios
  - **SP 3.2:** Establish a Definition of Required Functionality and Quality Attributes
  - **SP 3.3:** Analyze Requirements: finding the necessary and sufficient requirements.
  - **SP 3.4:** Analyze Requirements to Achieve Balance
  - **SP 3.5:** Validate Requirements with simulation or prototyping

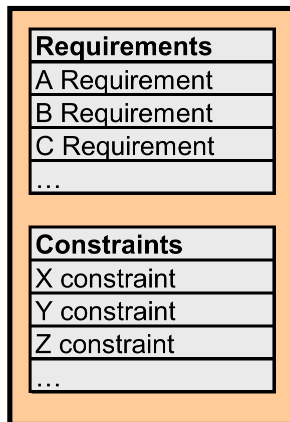
Requirements management

- **SG 1: Manage Requirements**
  - **SP 1.1:** Understand Requirements
  - **SP 1.2:** Obtain Commitment to Requirements
  - **SP 1.3:** Manage Requirements Changes
  - **SP 1.4:** Maintain Bidirectional Traceability of Requirements
  - **SP 1.5:** Ensure Alignment Between Project Work and Requirements

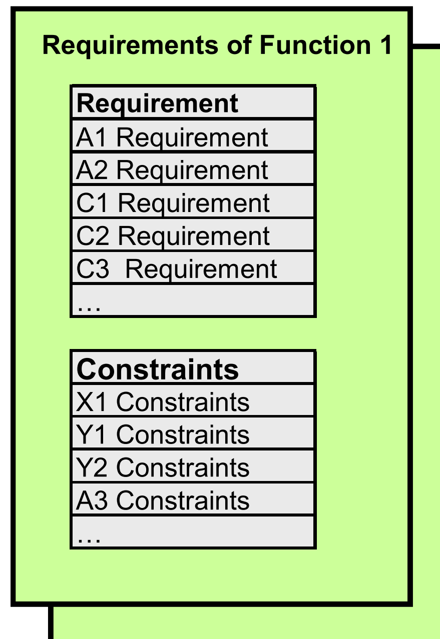
Typical tools are Excel or specific tool like DOORS

Requirements management

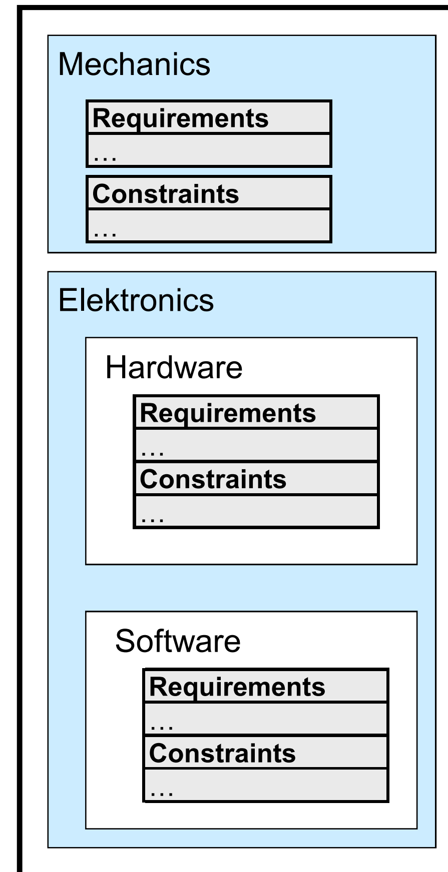
User Requirements



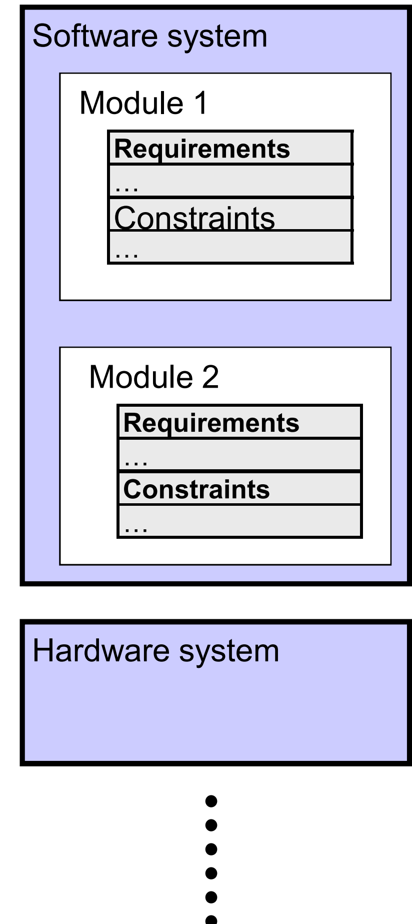
Logical System Architecture



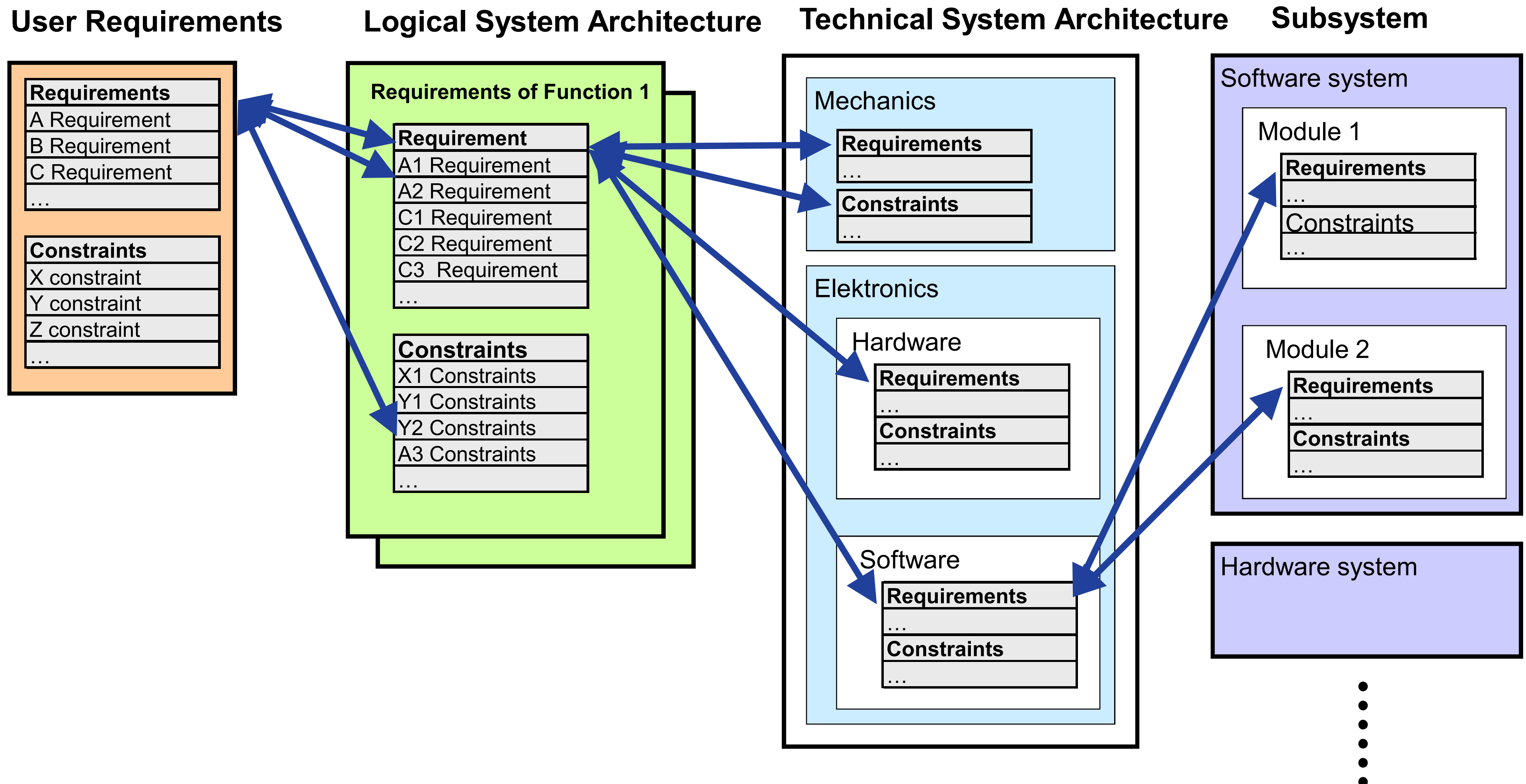
Technical System Architecture



Subsystem



Requirements management

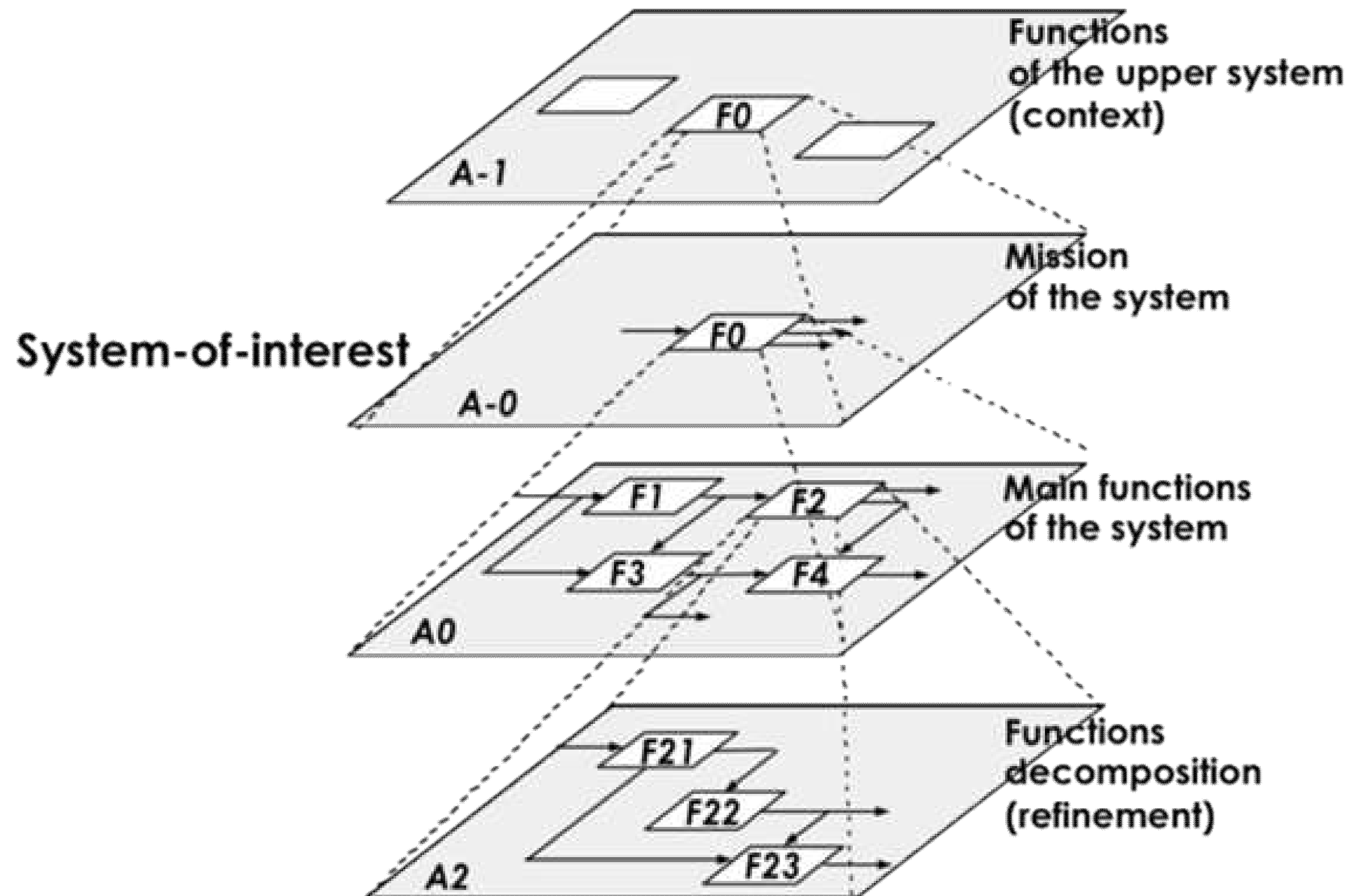


Logical System Design

Specification of logical system architecture

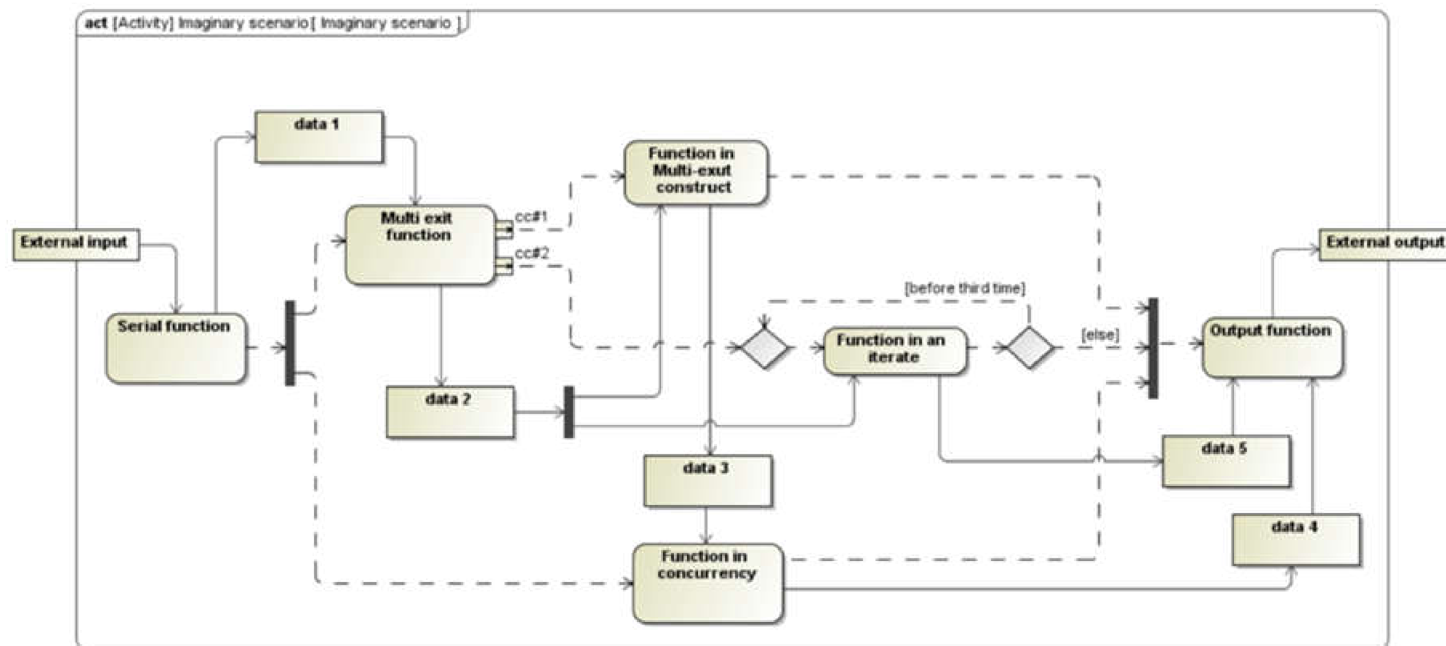
- Goal is to divide the device into components
  - What are the main logical components, blocks?
  - What is the connection between the main logic blocks?
- Analyzing the data path between the input and the output
  - How is the output created from the input?
  - What are the main stages?
- There are many types of Logical architecture representation
  - Static view: functions and their interconnections
  - Dynamic view: Data flow of an incoming data
- There are no strict restriction for creating the logical architecture, mainly this is some kind of art requiring much experience

Specification of logical system architecture



Specification of logical system architecture

- Most widespread technics and tools
  - structured analysis design technique
  - Functional Flow Block Diagrams
  - UML, SysML diagram



Designing of Technical System Architecture

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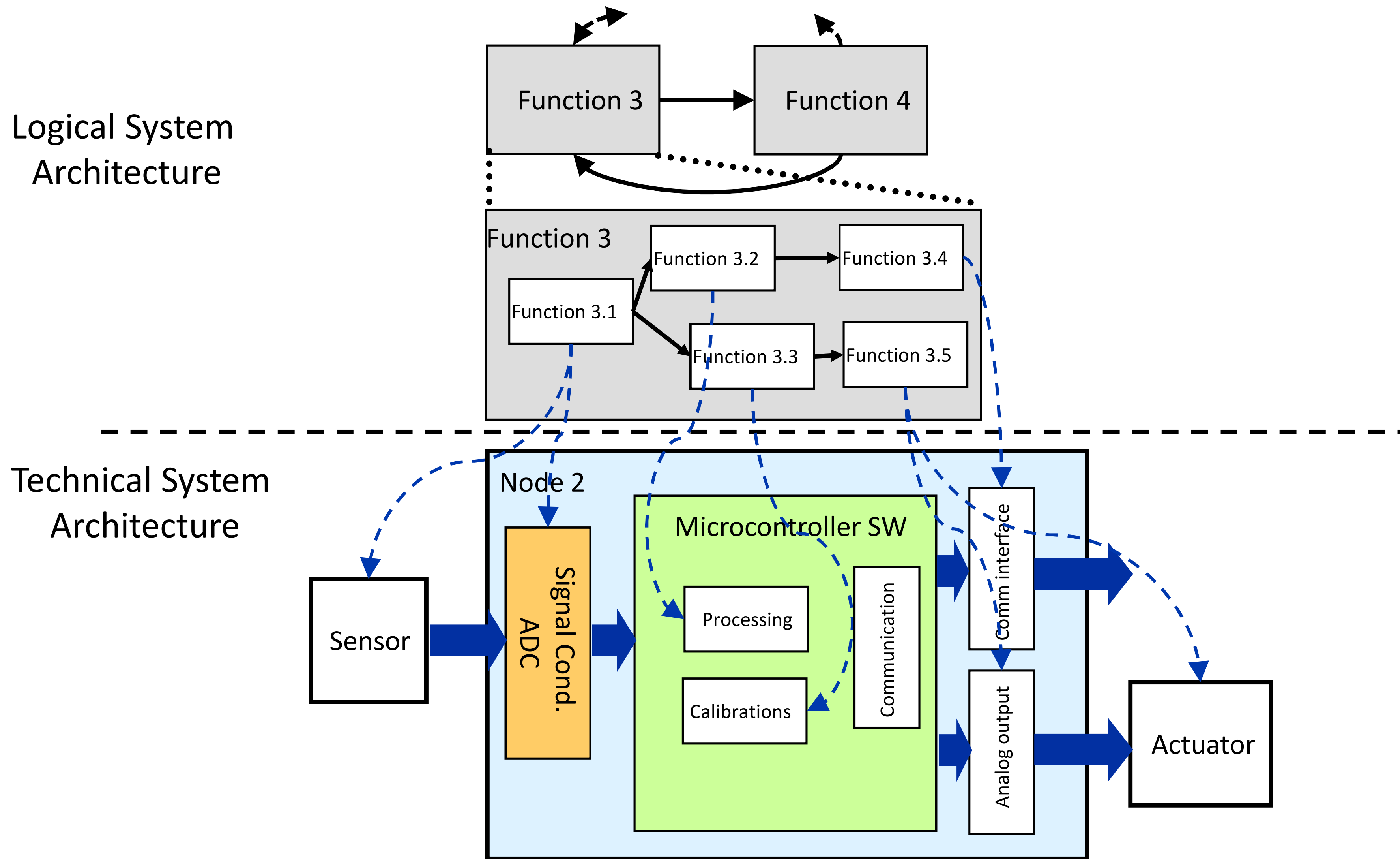
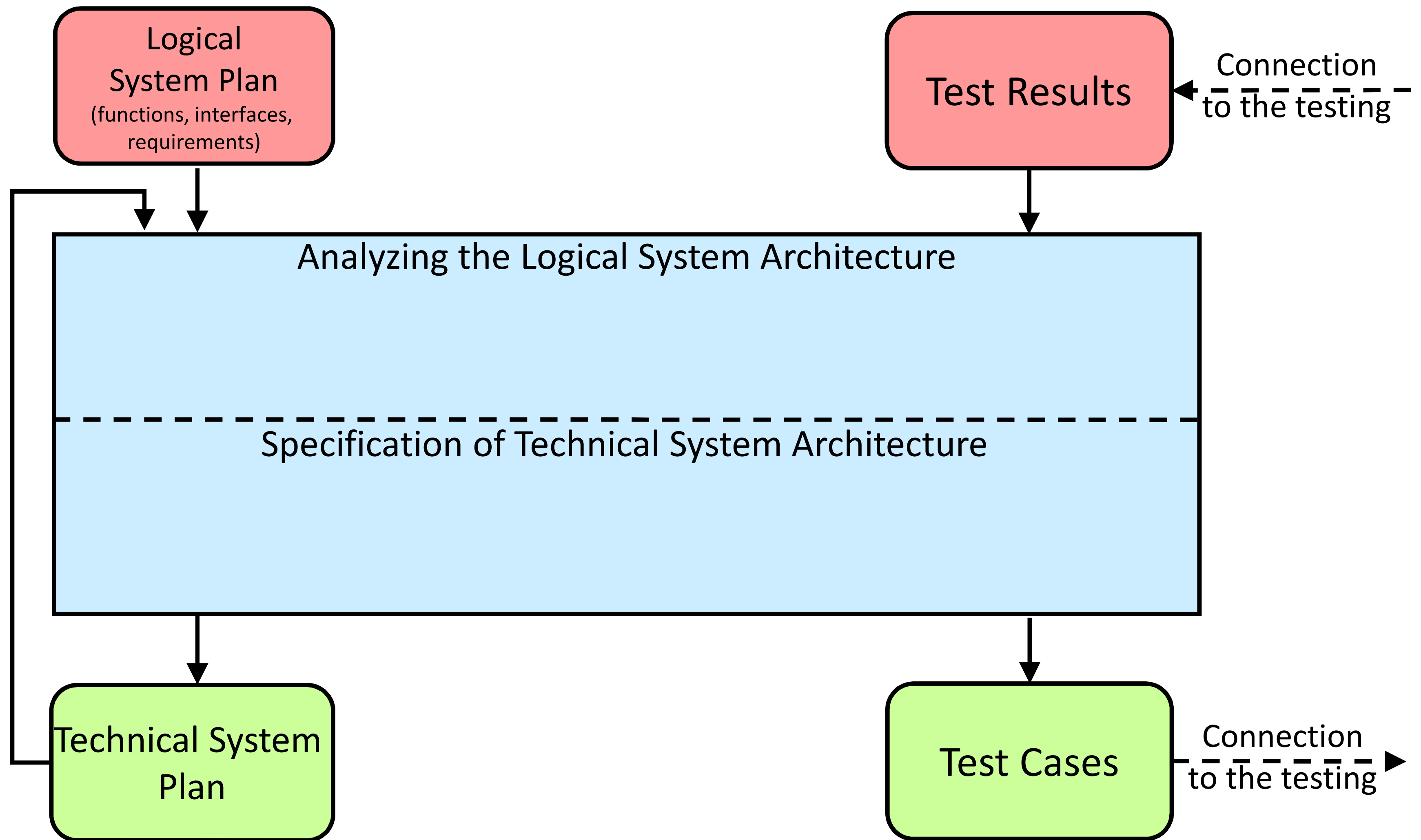
Analyzing logical system architecture, specification of the technical system architecture



Analyzing of Logical System Arch. Specification of Technical System Arch.



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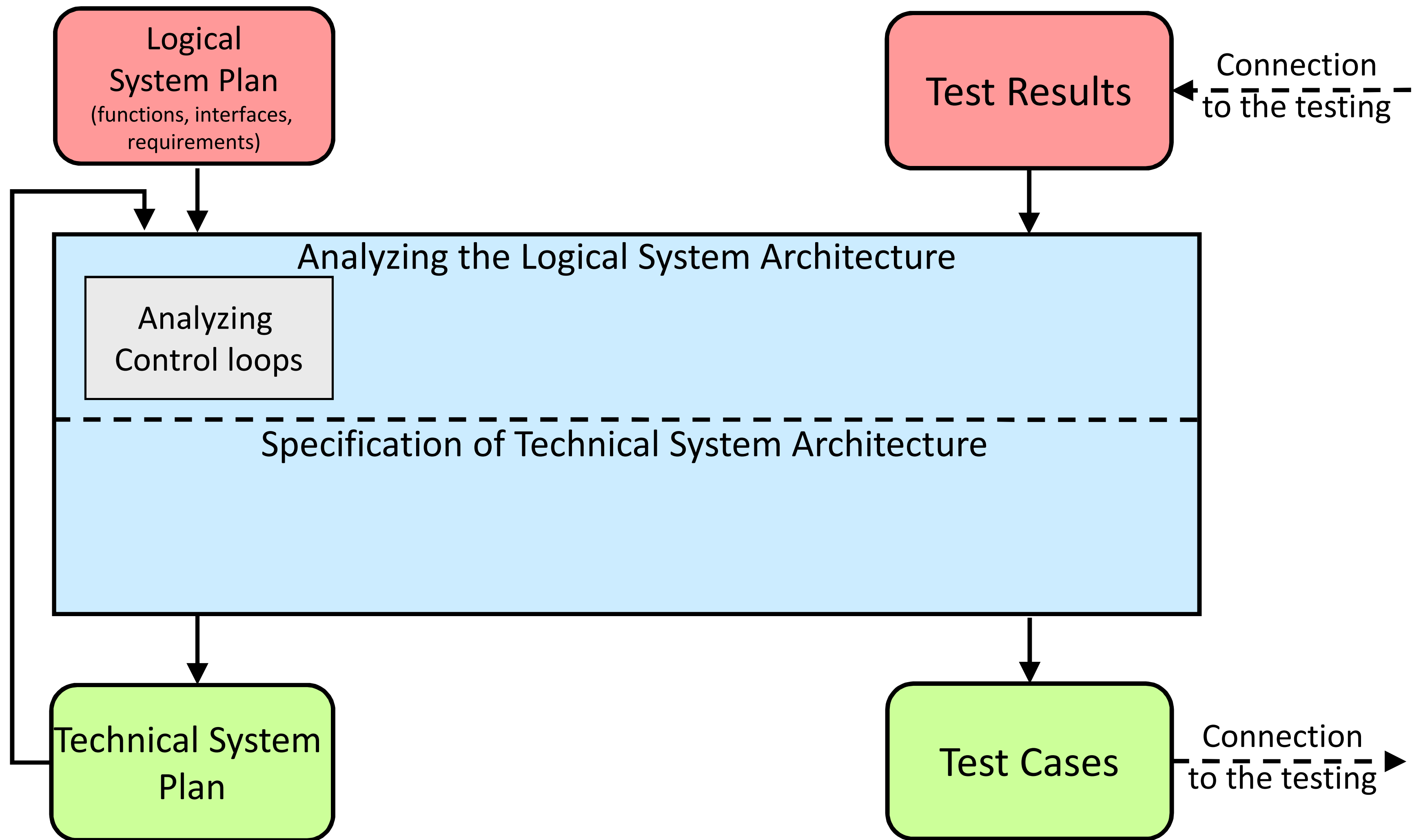
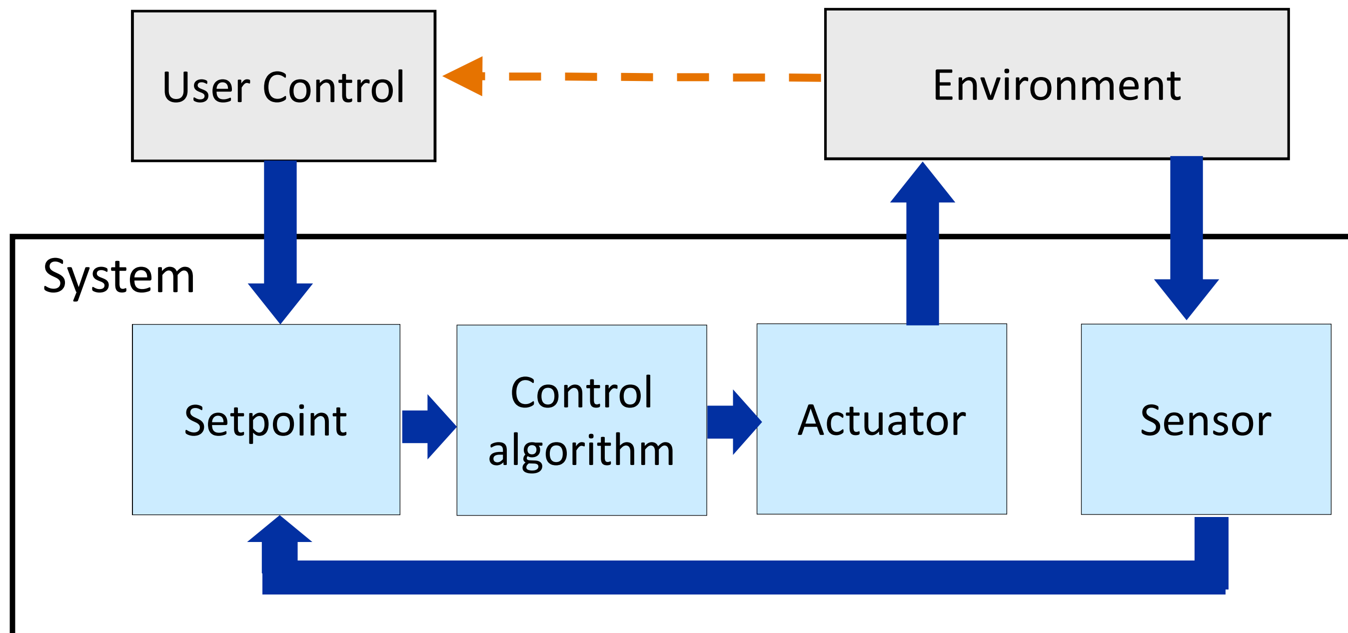


Analyzing Control loops



Analyzing Control loops information can be gathered

- Types of internal and external interfaces
- The required precision and granularity of signals
- Prediction on timing
- Prediction on required processing capability
- Prediction on physical constraints and layout

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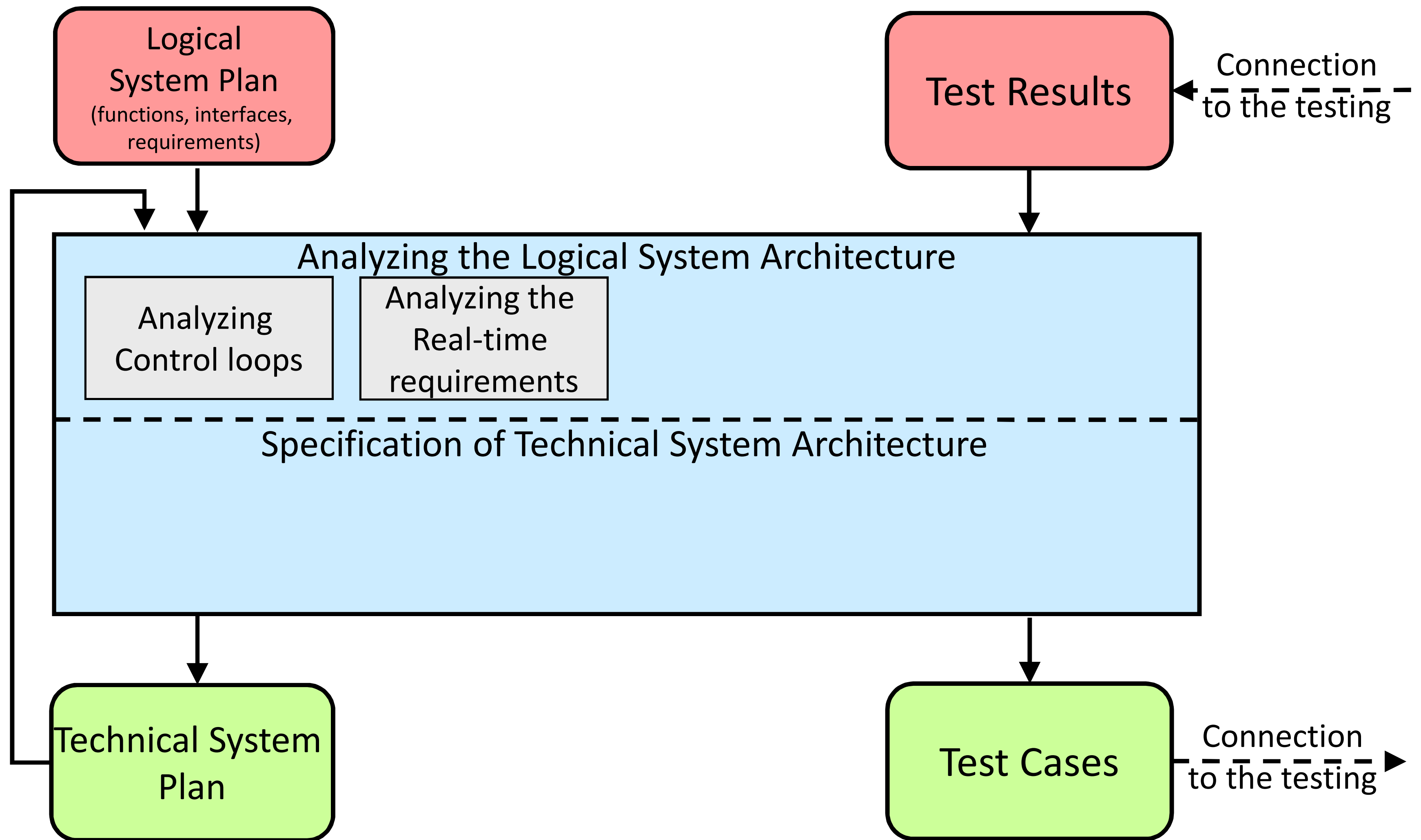
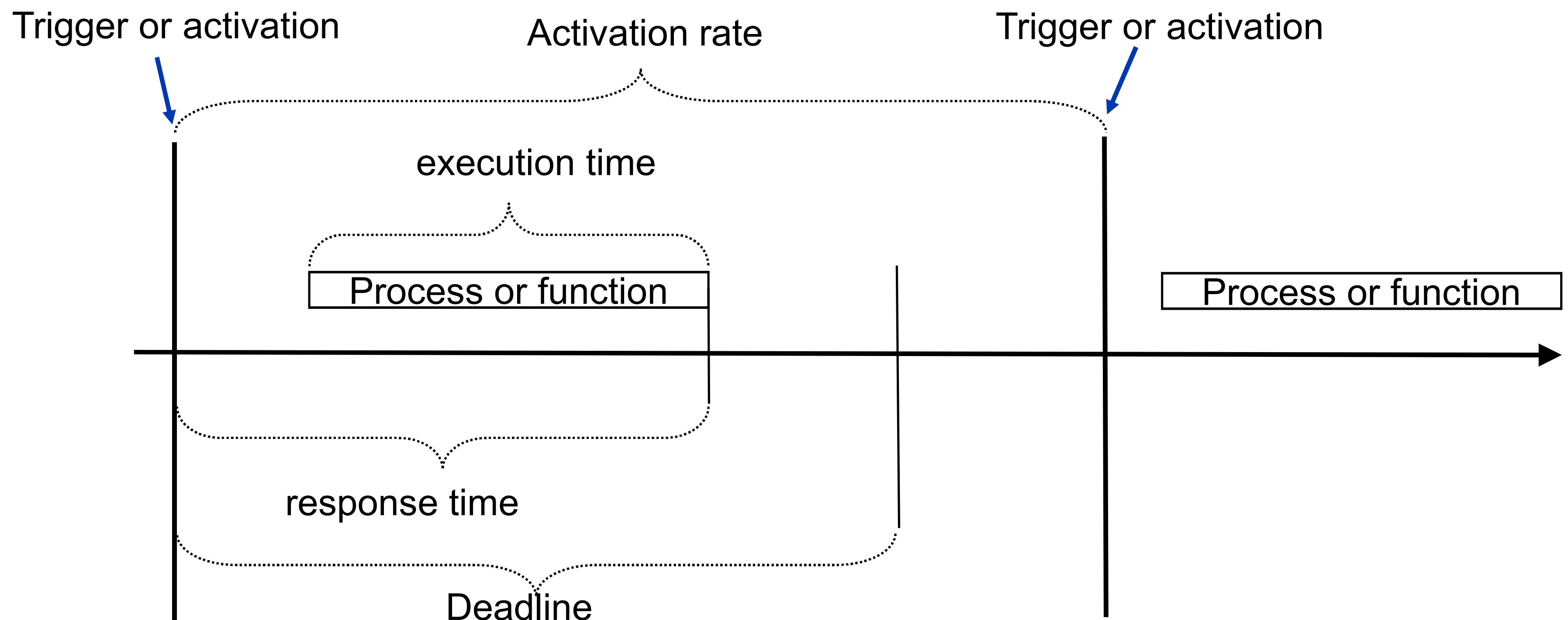
Analyzing of Logical System Arch.
Specification of Technical System Arch.

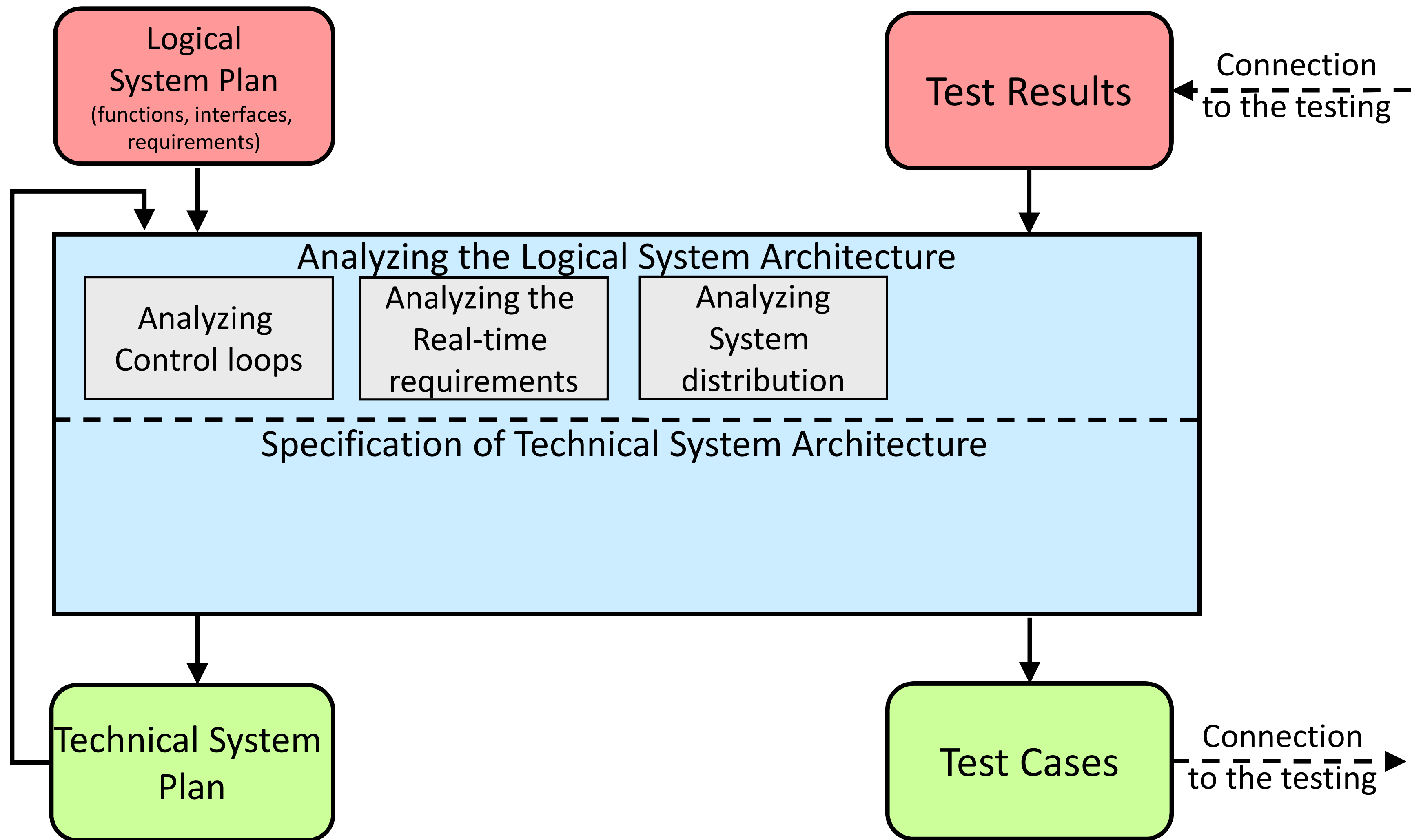


Predictions and requirements on Real-time characteristics

- Determining system level real-time requirements
- Allocating timing requirements to functions



Analyzing of Logical System Arch. Specification of Technical System Arch.



Analyzing Distributed System Functions

- What functions need to be encapsulated into one device, or separated into different devices?
  - Processing capacity
  - Timing
  - Physical layout
- What type of communication connection needed between devices
  - Bandwidth
  - Range
  - Communication Technology
- Designing of the communication matrix
  - Messages
  - Signals and their encodings

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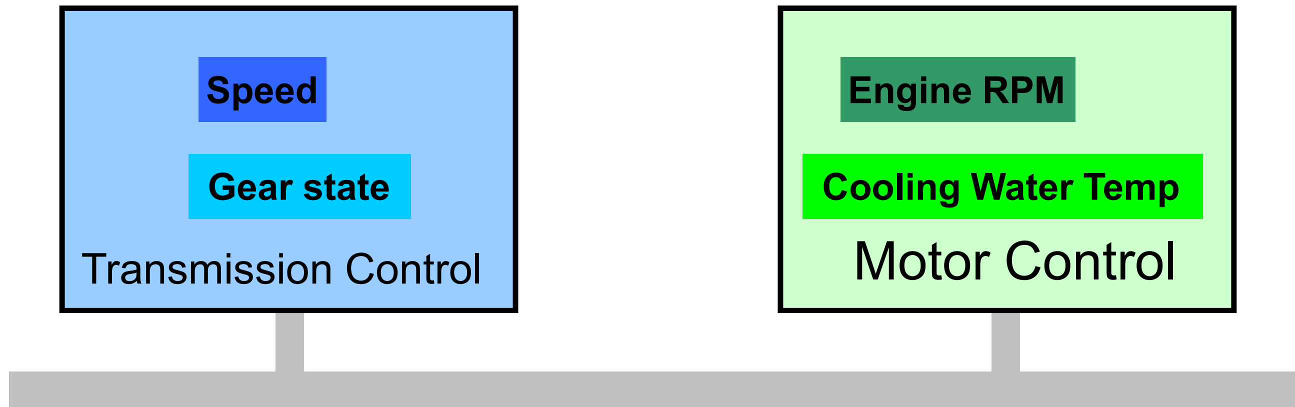
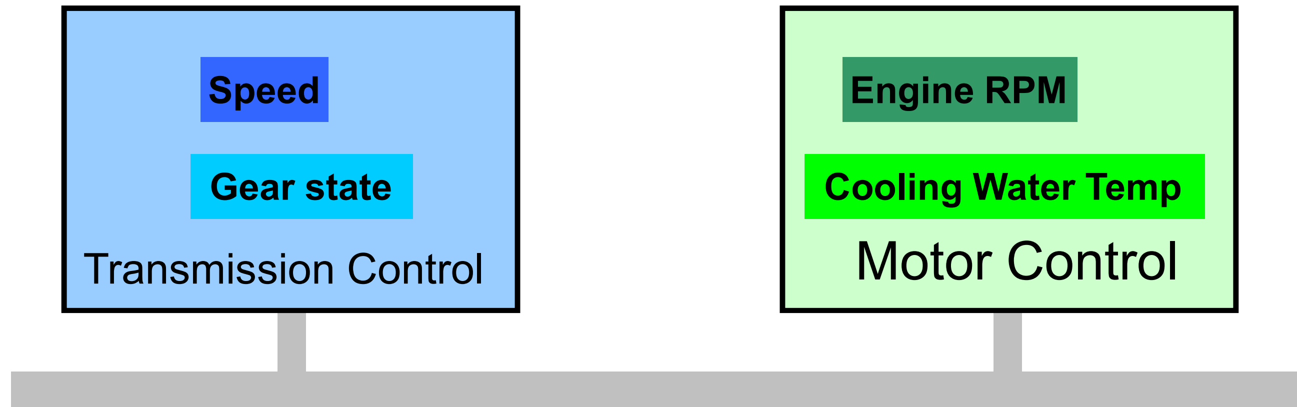
Signal example



Signal name	Min-max	Unit
Speed	0 – 250	km/h
Gear state	-1 – +5	
Engine RPM	0 – 10000	RPM
Cooling Water Temp	-20 – 100	C degree

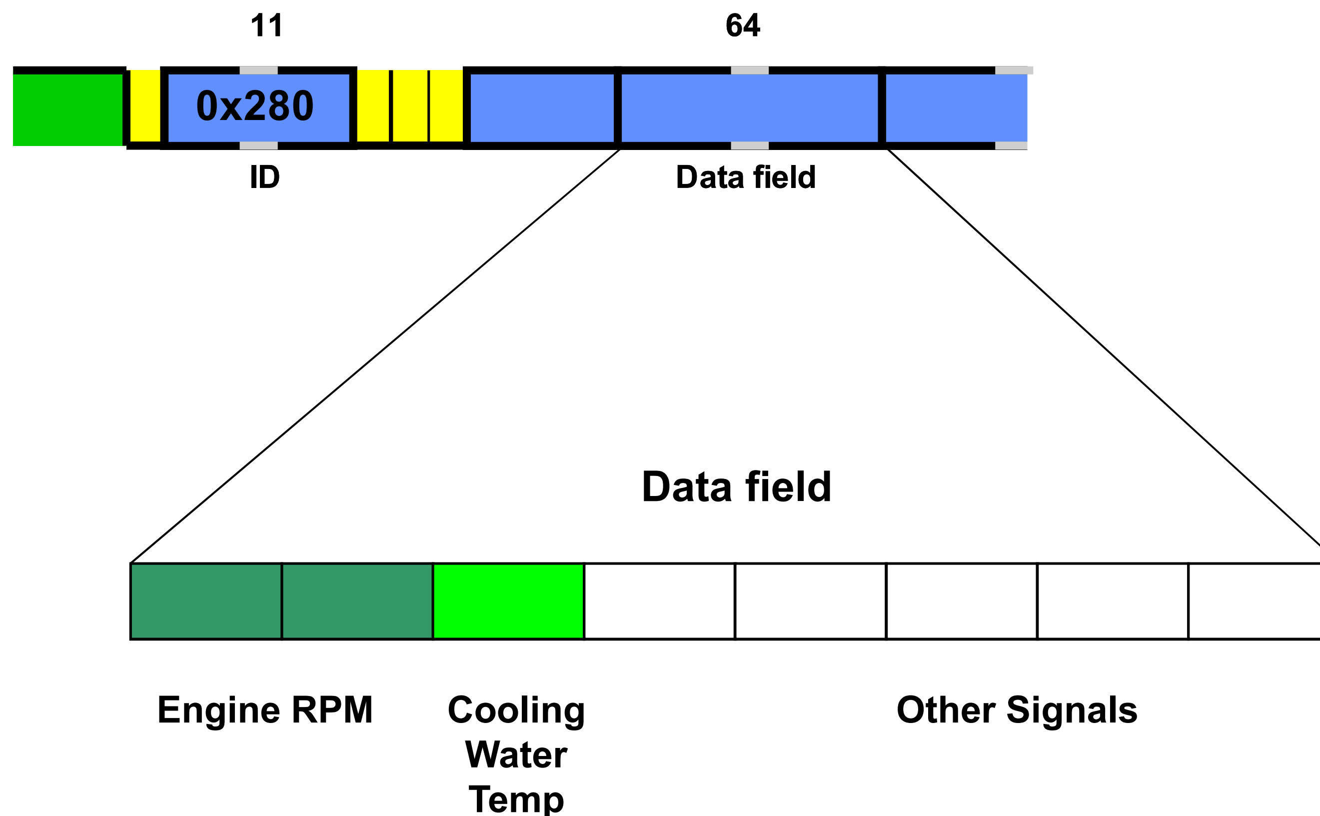
Signal, example



Signal name	Min-max	Unit	Conversion	Data size
Speed	0 – 250	km/h	y = x * 4	10 bit
Gear state	-1 – +5		y = x + 1	3 bit
Engine RPM	0 – 10000	RPM	y = x	16 bit
Cooling Water Temp	-20 – 100	C degree	y = (x+20) * 2	8 bit

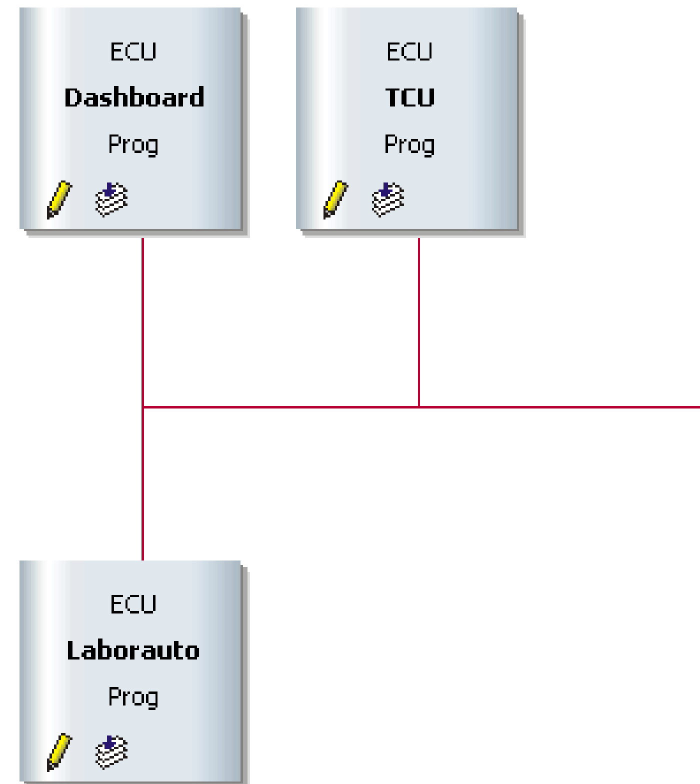
Messages and signals

Engine parameters message, ID=0x280



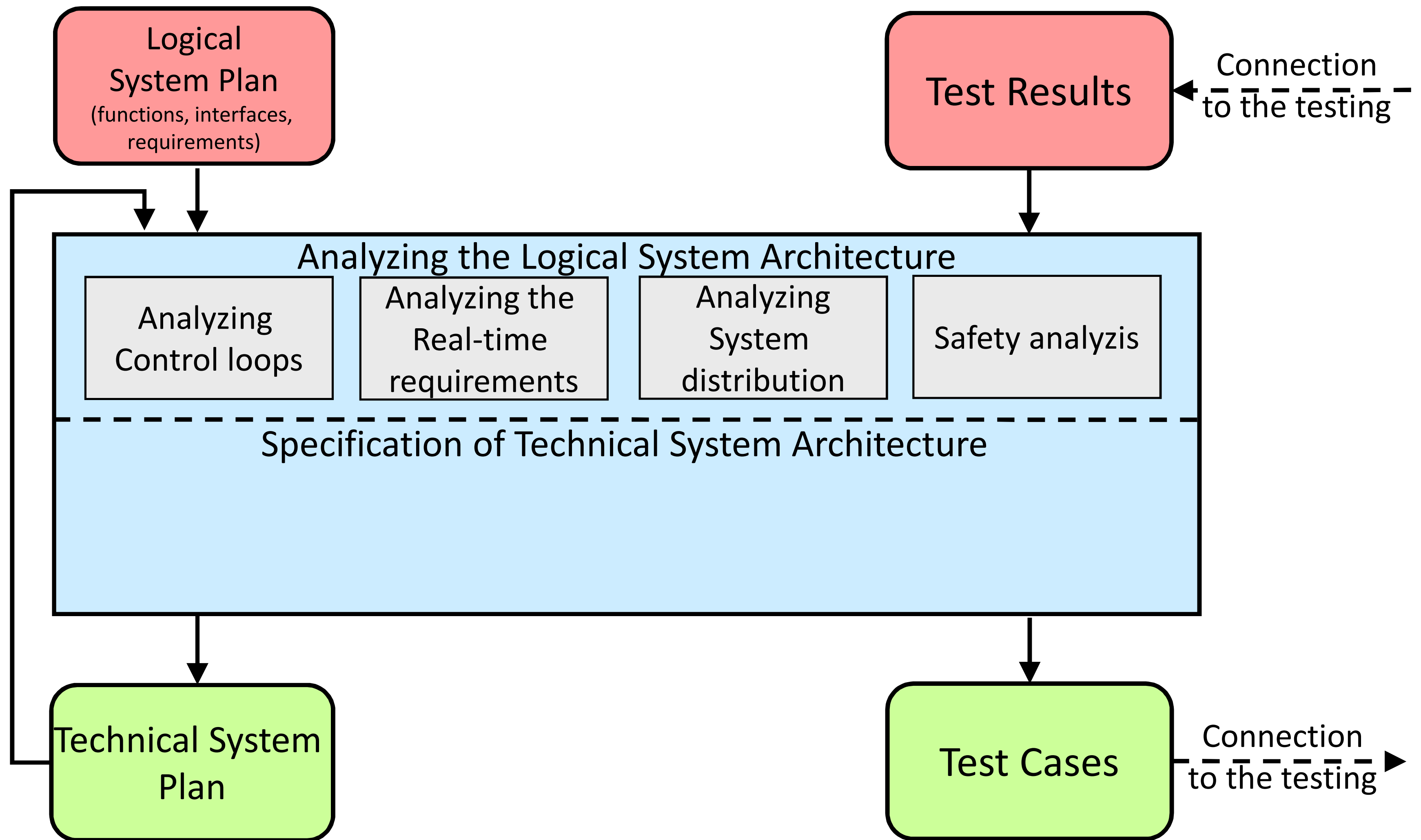
Communication matrix

- Vector CANdb editor
  - 4 message
  - 5 signals

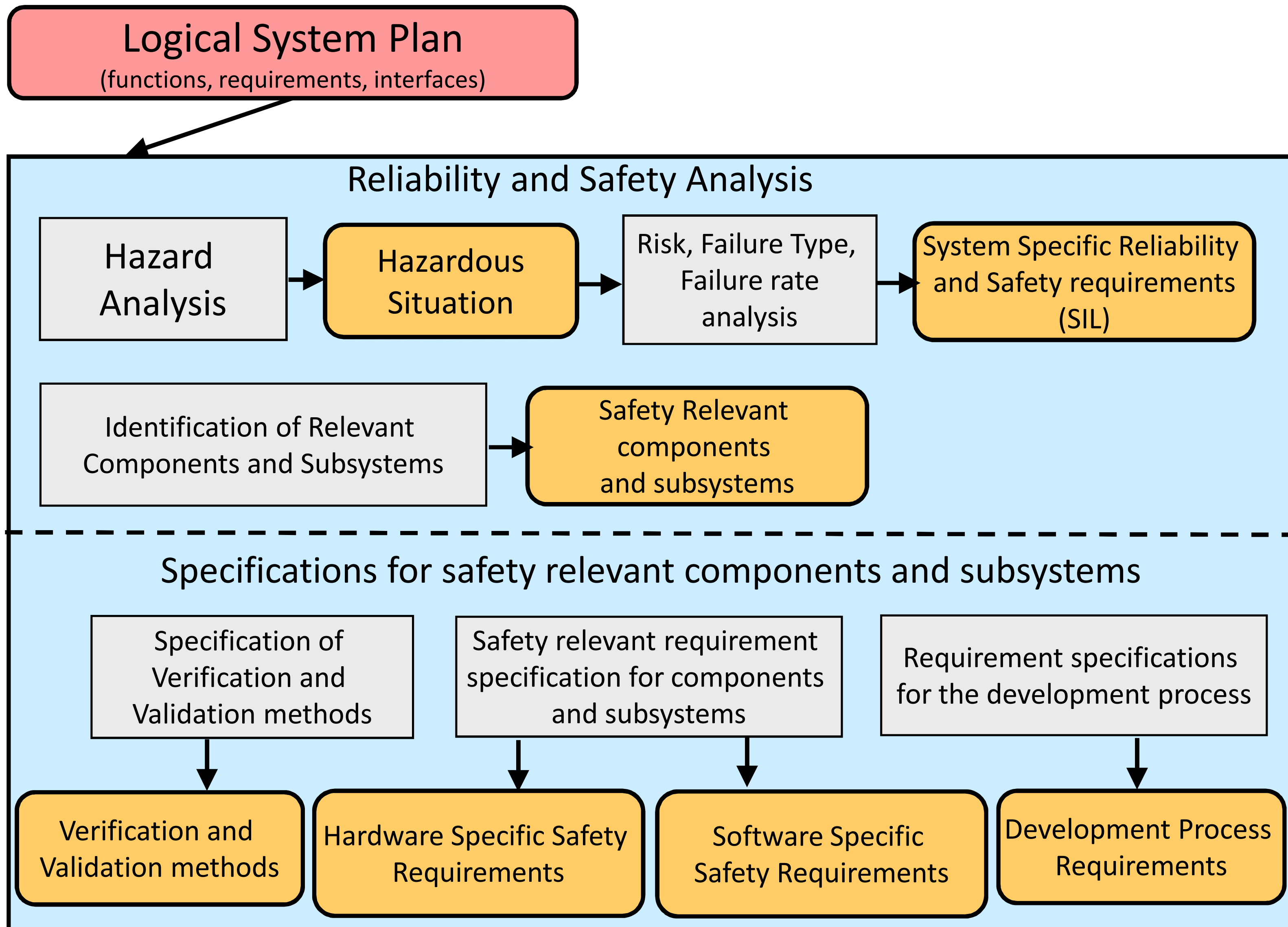


Signals/Node	TCU	Laborauto	Dashboard
accelerator_pedal	AcceleratorPedal_Coolant (0x380)	<Tx> AcceleratorPedal_Coolant (0x380)	
coolant_temp	AcceleratorPedal_Coolant (0x380)	<Tx> AcceleratorPedal_Coolant (0x380)	AcceleratorPedal_Coolant (0x380)
Gear_state	<Tx> Gear (0x440)	Gear (0x440)	
speedometer		<Tx> Dashboard (0x5A0)	Dashboard (0x5A0)
tachometer	MotorParameter (0x280)	<Tx> MotorParameter (0x280)	MotorParameter (0x280)

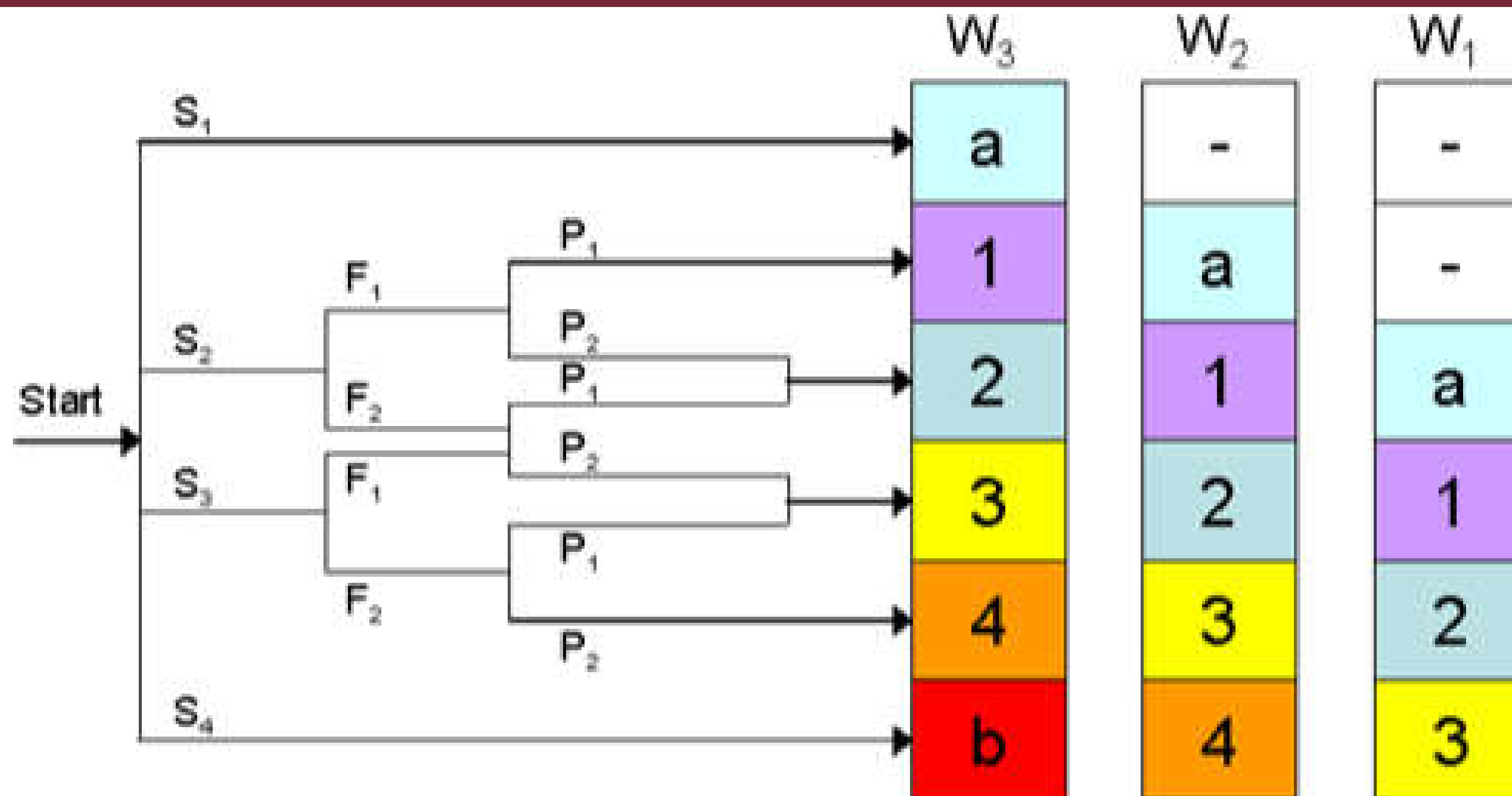
Analyzing of Logical System Arch. Specification of Technical System Arch.



Safety analysis



Safety Integrity Levels



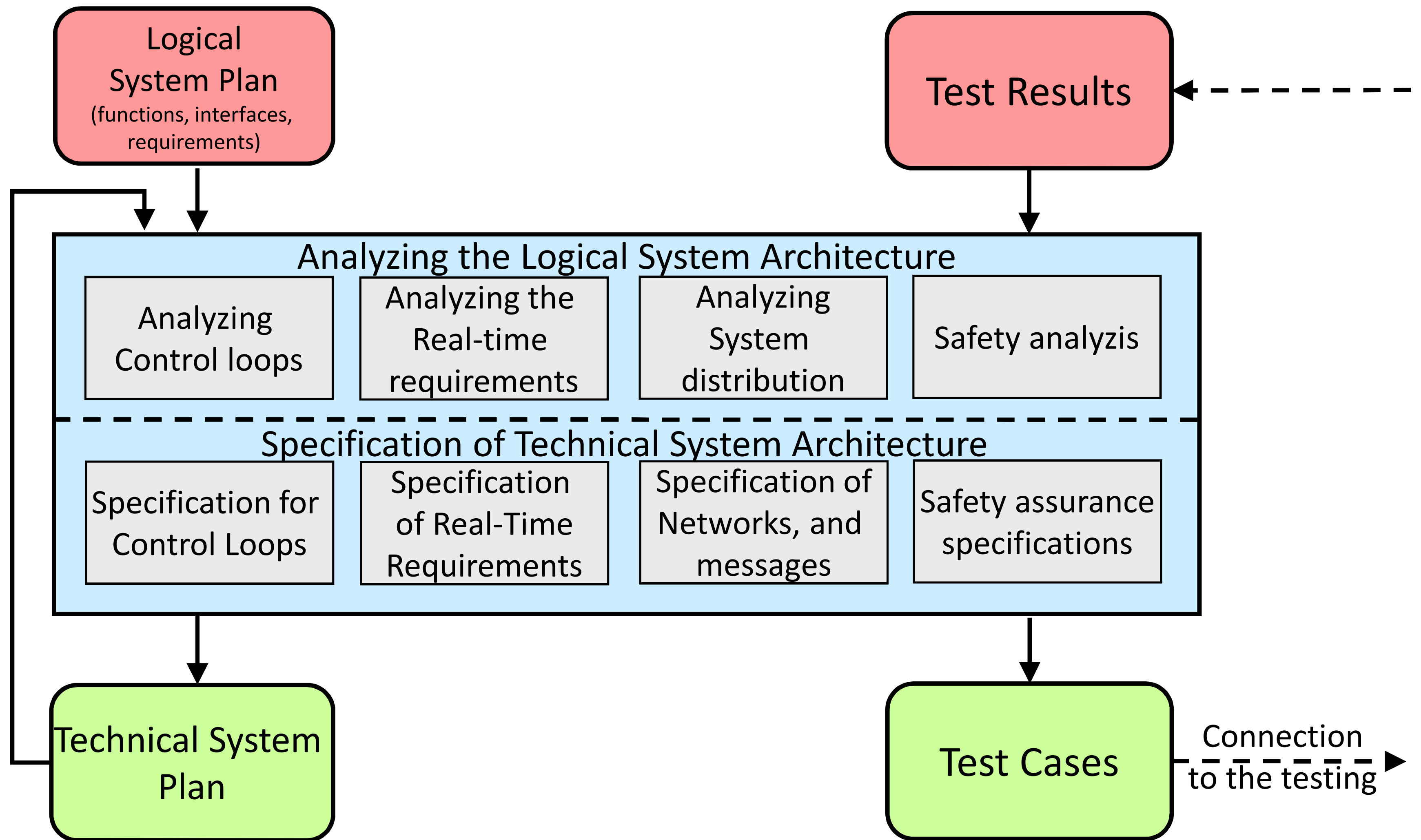
Ref	Description
-	No requirement
a	No special requirement
1,2,3,4	Safety Integrity Level (SIL)
b	A single SIS is not sufficient

Affects of SIL layers to the development

- SIL layers, or other Safety Levels give restictions for every step of development process
  - Design
  - Implementation
  - Testing

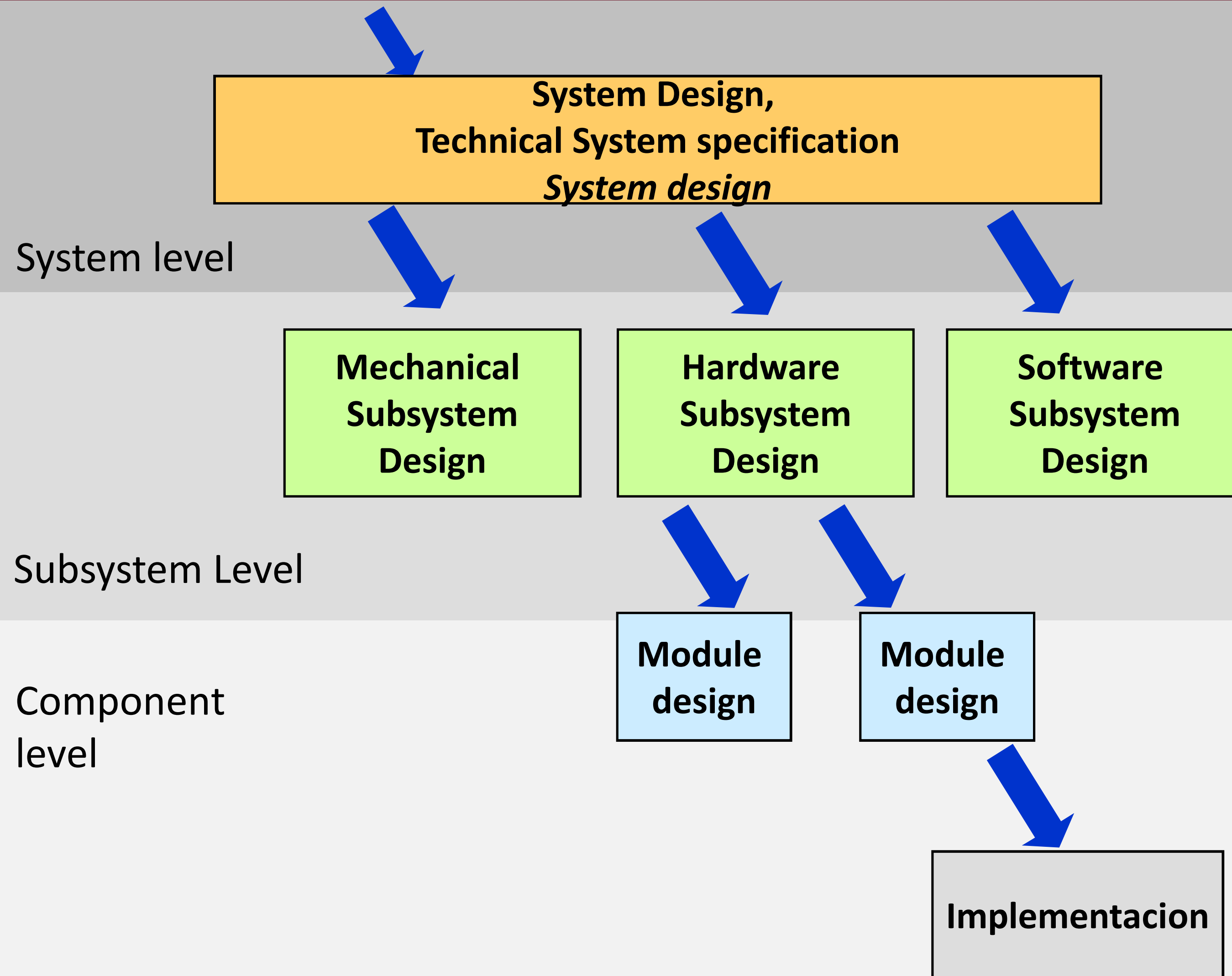
Activity	SIL0	SIL1	SIL2	SIL3
Independent review of functional requirements	+	+	++	++
Prototyp	0	0	+	++
Simulation	+	+	++	++
FMEA (Failure Mode and Effect Analysis)	+	+	+	++
Statement Coverage	+	++	++	++
Decision Coverage	+	+	+	++

Analyzing of Logical System Arch. Specification of Technical System Arch.



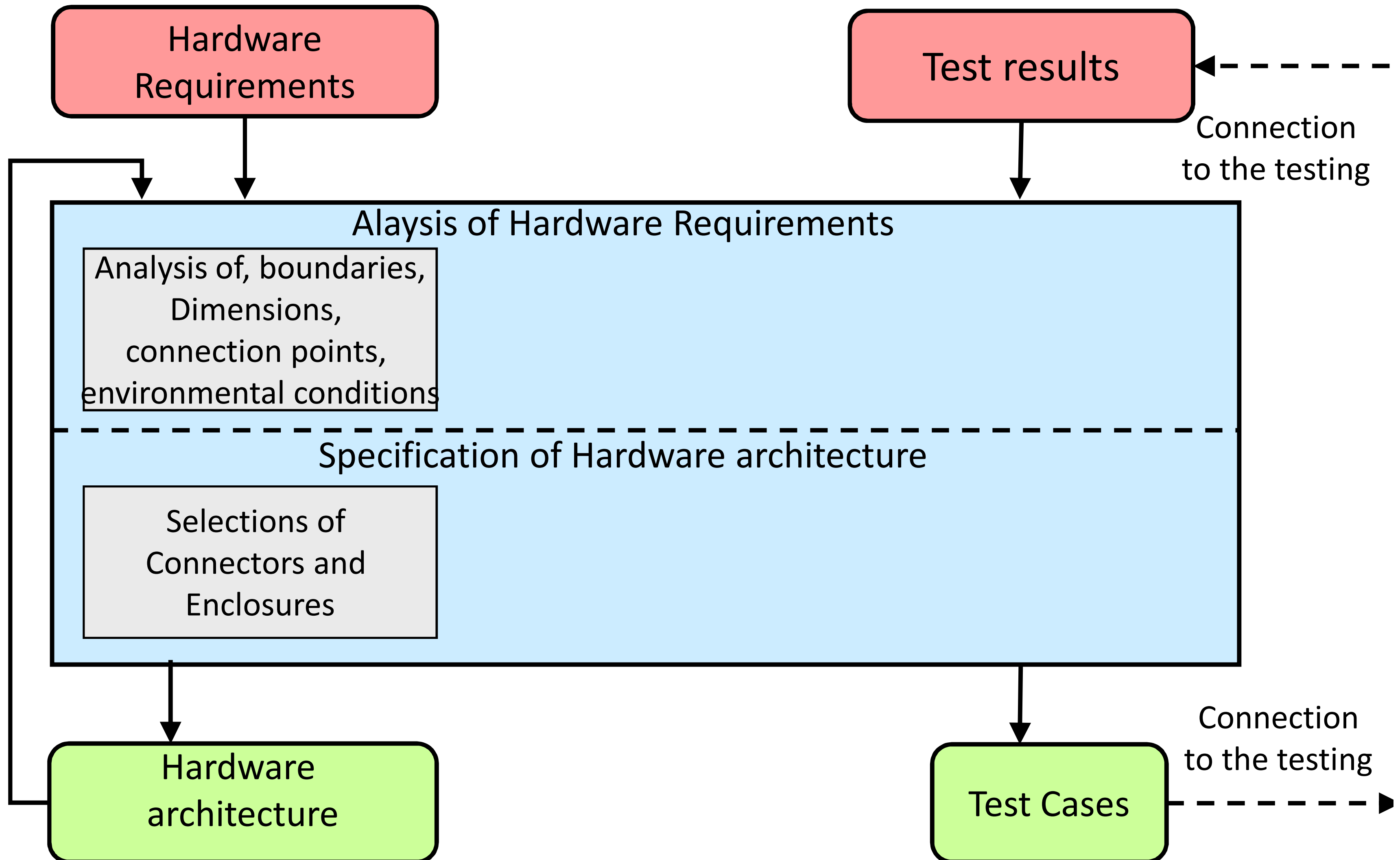
Branching to subsystem paths

Branching to subsystem paths – Electronics *(Hardware – Software)* path



Hardware Design Path

Hardware Architecture Design



Analysis of boundaries, dimensions, connection points, environmental conditions

- Mostly there are predetermined mechanical constraints
  - Dimensions
  - Weight
  - Usable areas, and usable component type (for example because of vibrations)
- Selection of Enclosure and Connectors
  - Determines the dimension and useable areas of the PCB
  - Environmental conditions should be taken into account: IP protection, enclosure type

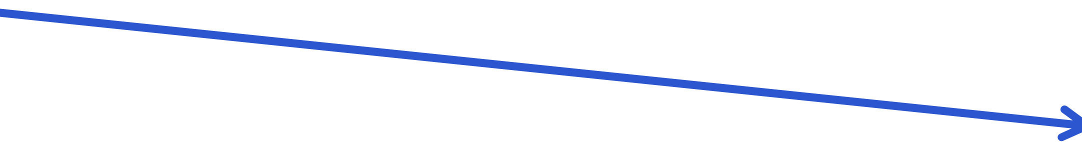
Properties of Enclosures and Connectors

- Enclosure
  - IP (Ingress Protection)
  - Protection against physical impacts
  - UV radiation protection
  - Chemical protection
  - RF, and magnetic shielding
  - Heat conductance
  - PCB mounting positions
  - Enclosure mounting options

- Connectors
  - Voltage, and current limits
  - Number of connections
  - Vibration protection
  - Shielding
  - IP (Ingress Protection)

IP (Ingress Protection)

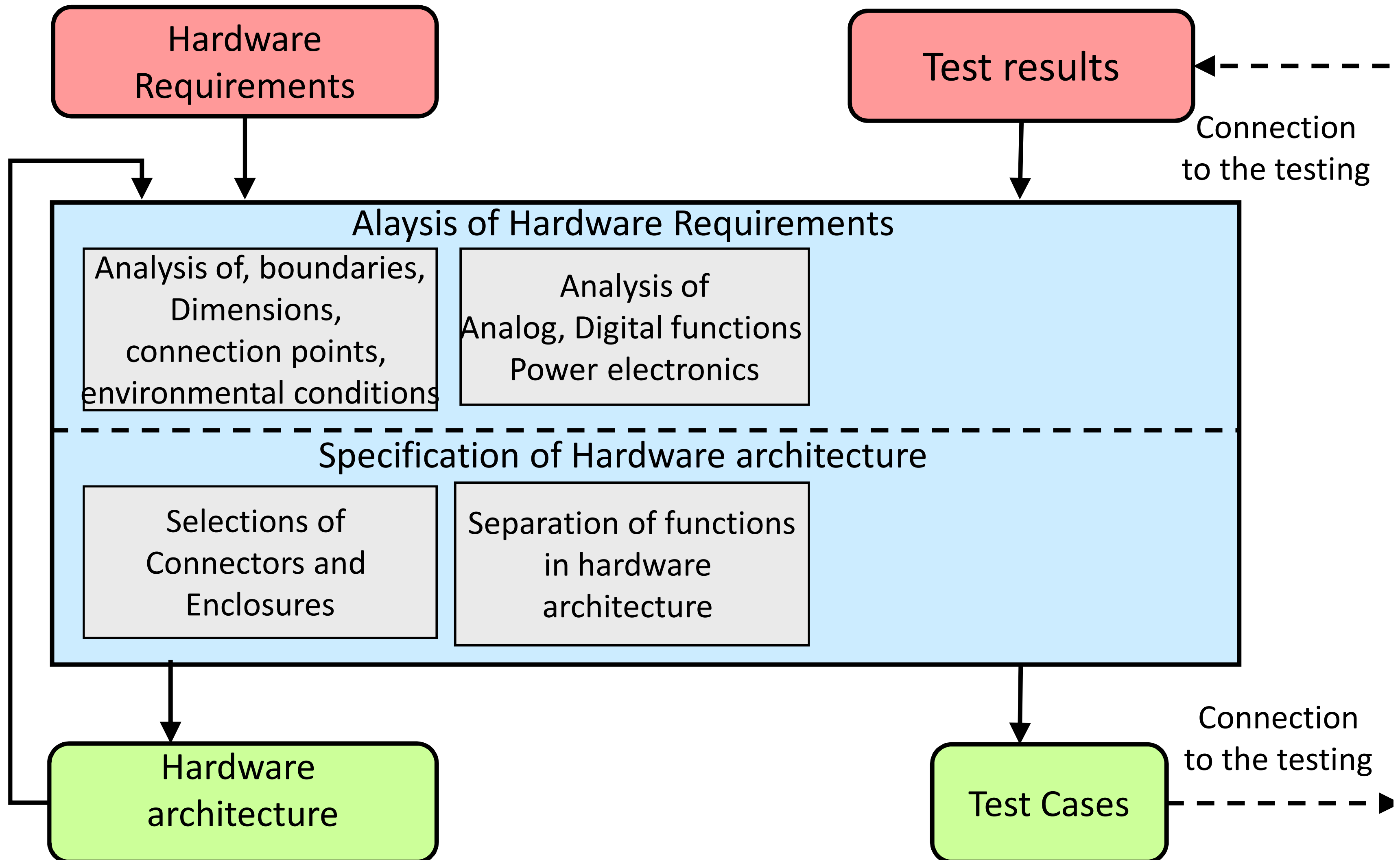
- IP 65



Solid particle protection		
Level sized	**Effective against**	**Description**
0	—	No protection against contact and ingress of objects
2	>12.5 mm	Fingers or similar objects
3	>2.5 mm	Tools, thick wires, etc.
4	>1 mm	Most wires, slender screws, large ants etc.
5	Dust protected	Ingress of dust is not entirely prevented, but it must not enter in sufficient quantity to interfere with the satisfactory operation of the equipment.
6	Dust tight	No ingress of dust; complete protection against contact (dust tight). A vacuum must be applied. Test duration of up to 8 hours based on air flow.

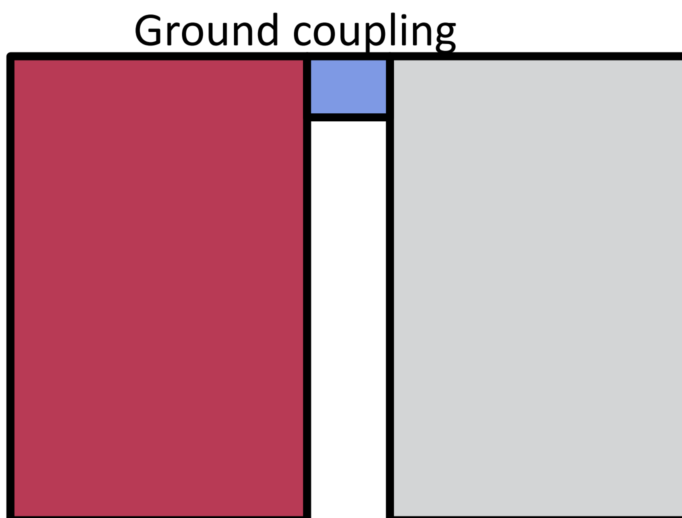
Water Protection	
Level	**Protection against**
0	None
1	Dripping water
2	Dripping water when tilted at 15°
3	Spraying water
4	Splashing of water
5	Water jets
6	Powerful water jets

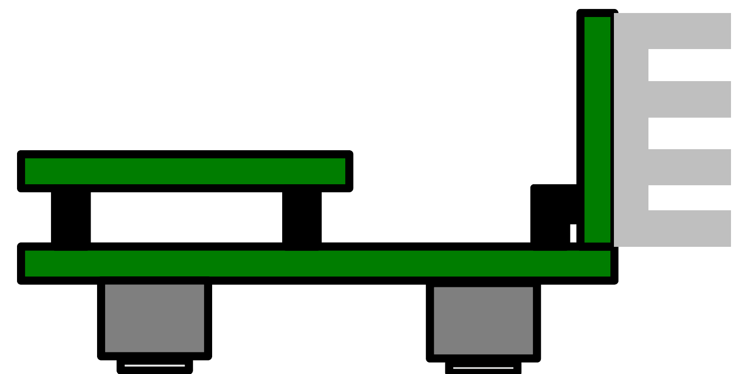
Hardware Architecture Design



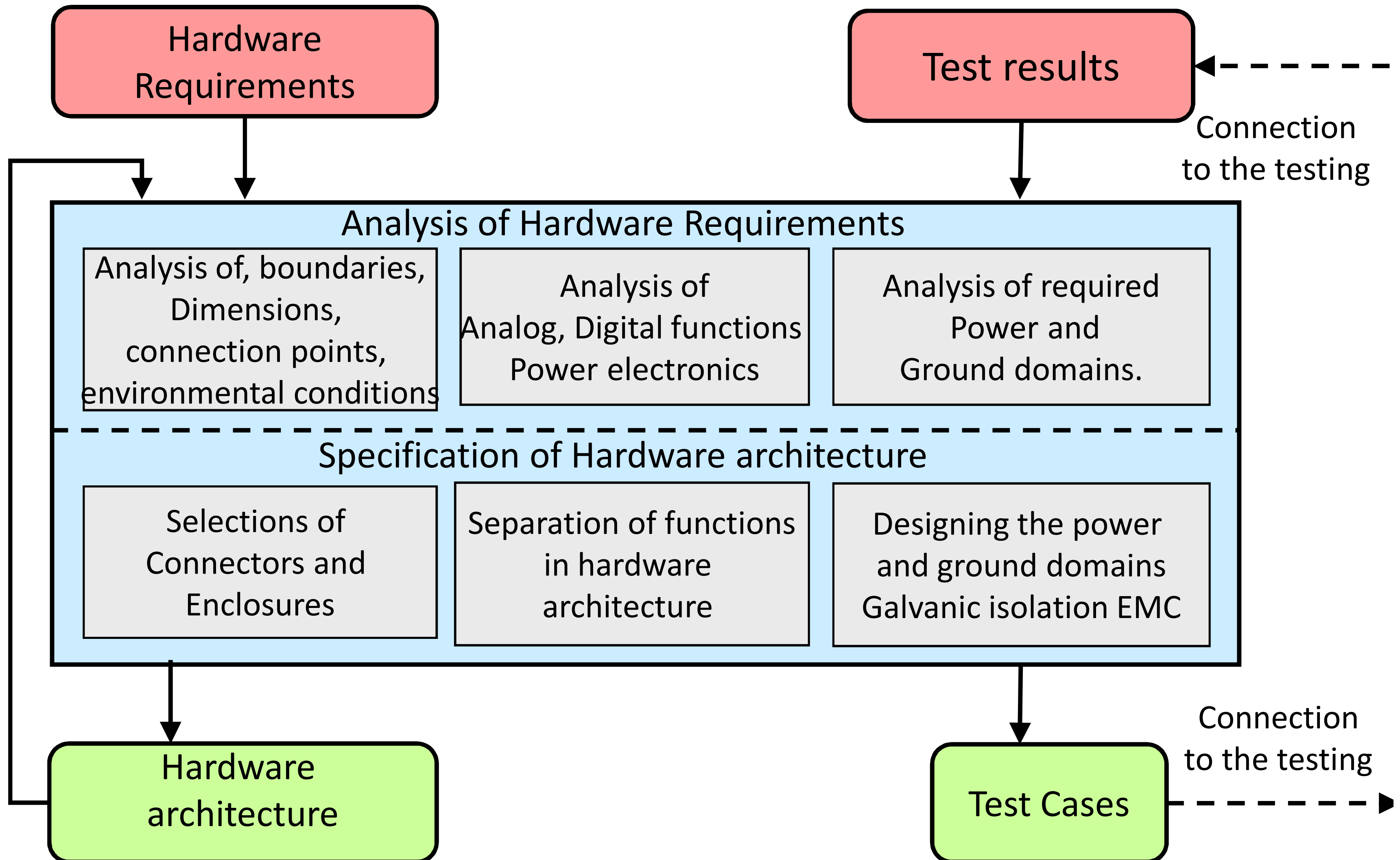
Separating the analog, digital and power electronics functions

- No necessary to different PCB
- Identifying the hardware and PCB blocks, and designing the interconnection between them.



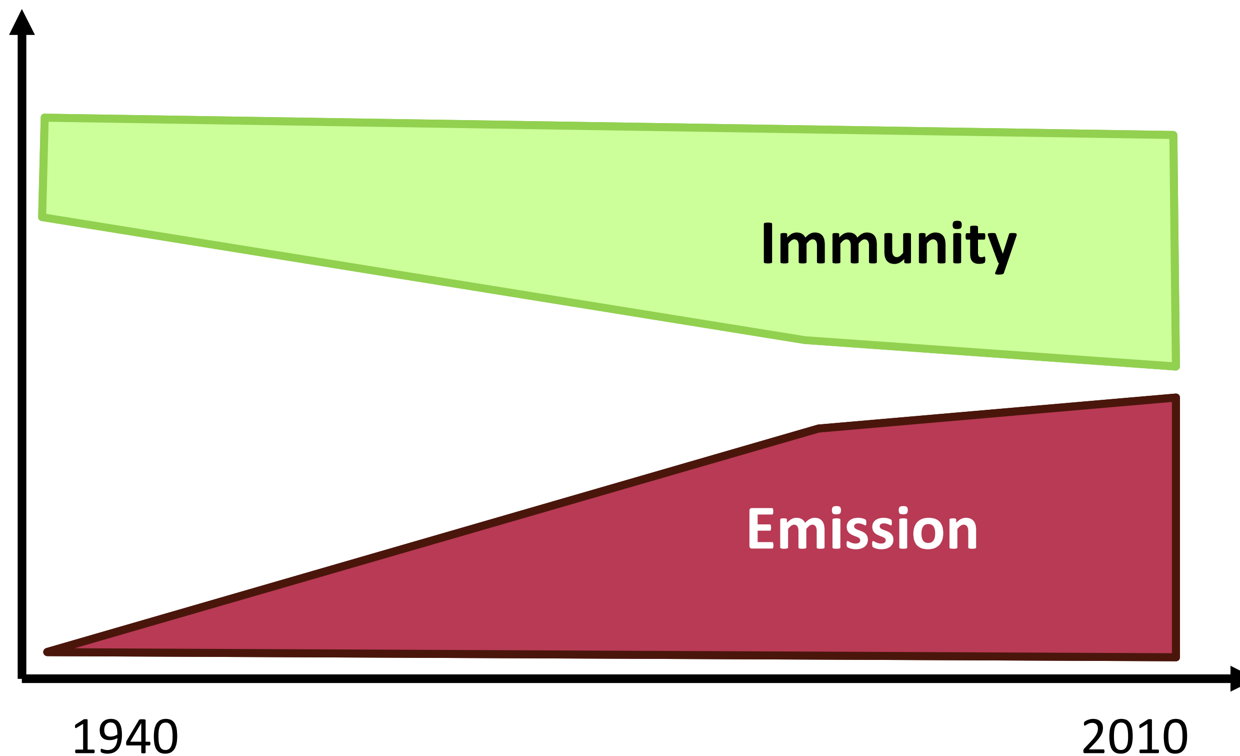


Hardware Architecture Design



EMC Electomagnetic Compatibility

- The EMC Gap is closing



Emission and Immunity

- Emission: more and more load to the environment
  - Harmonic emission
  - Conducted emission
  - Radiated emission
- Immunity: the ability of the device to resist the environmental noise
  - Conducted and radiated RF
  - Burst, Surge
  - Power supply line problems: voltage changes, voltage drop, period error
  - Magnetic field: sinus like change, non sinus like change
  - ESD Electro Static Discharge

Immunity classes

- **Class A**: The device keeps its measurement and functional specifications under the effect of environmental noises.
- **Class B:** The device is operational under the effect of environmental noises, but its measurement precision is effected by the noises.
- **Class C:** After the environmental noise an interaction from an operator is needed to make the device operational again.
- **Class D:** Data loss, functional problem or damage of the equipment is happen by the effect of the environmental noise

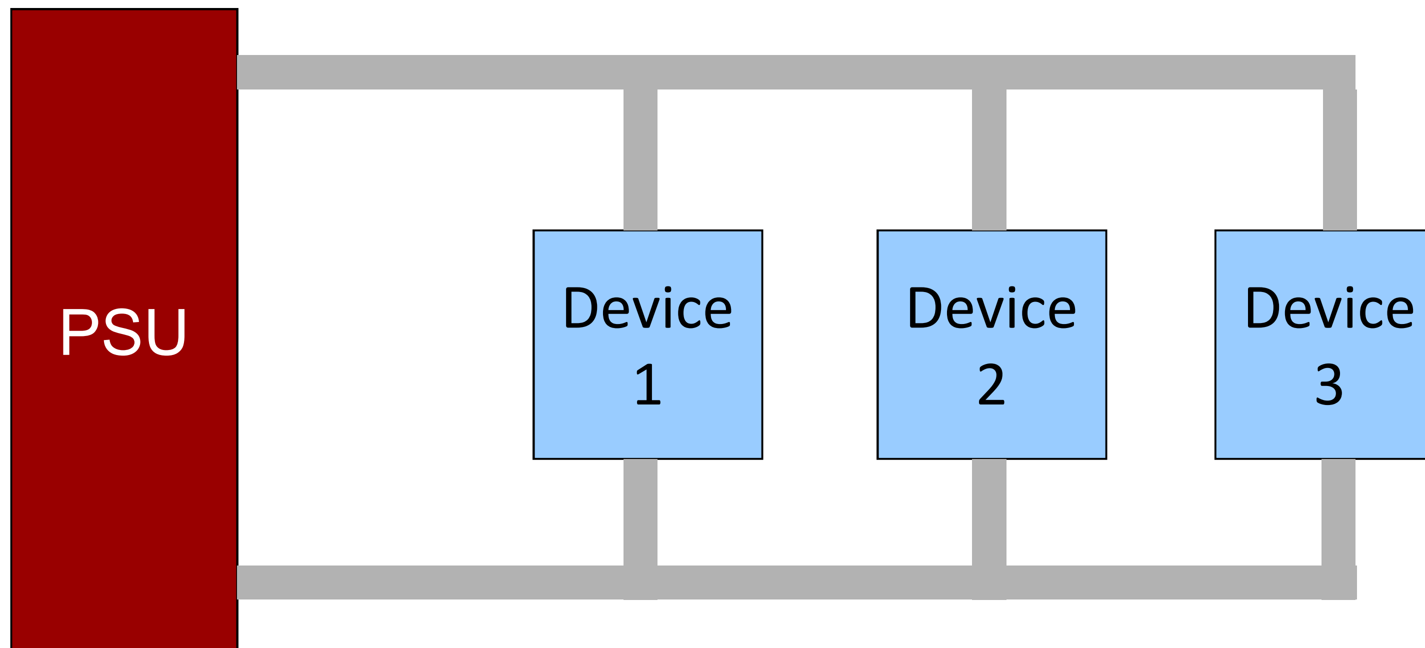
Inter or Intra system problems

- Inter System EMC
  - The noises emitted from the device to the environment
  - There are regularizations for this

- Intra System EMC
  - Noises that generated inside of the enclosure
  - Not regulated, but highly effects the operational ability of the device

Power supply architectures
Power bus

- Simplest, and the most problematic
  - Common impedance



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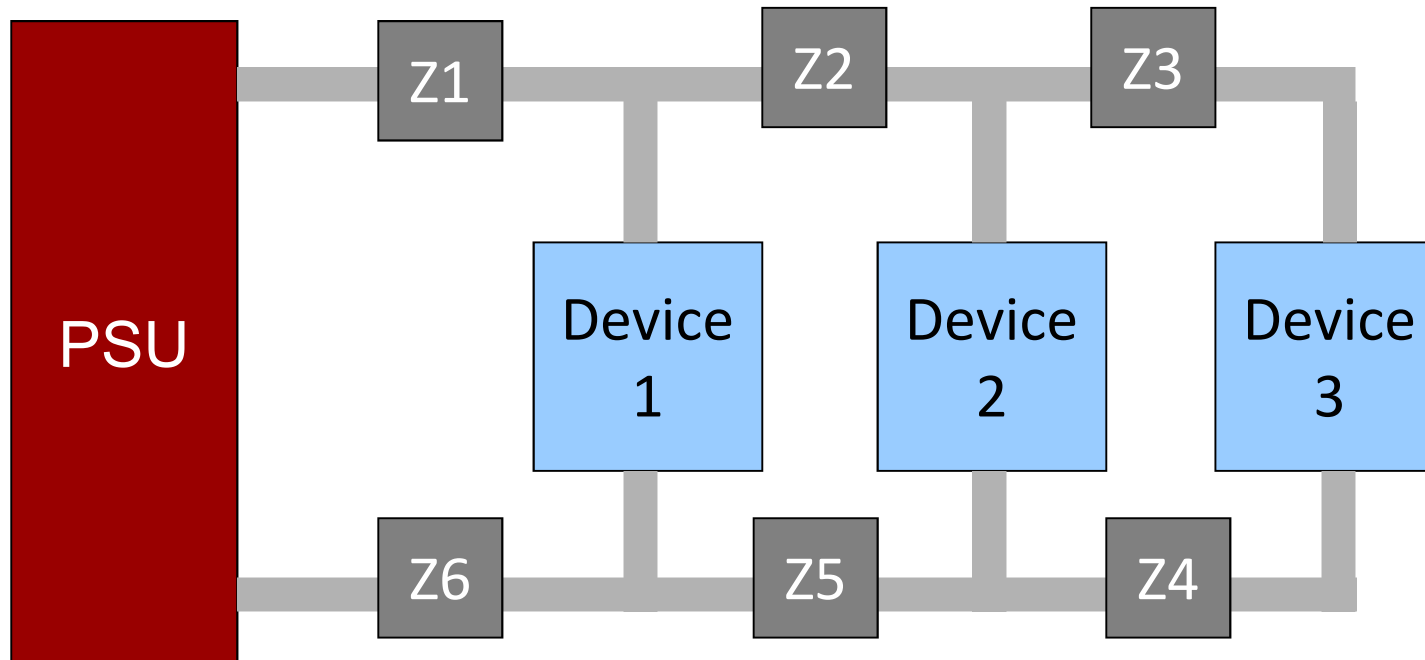

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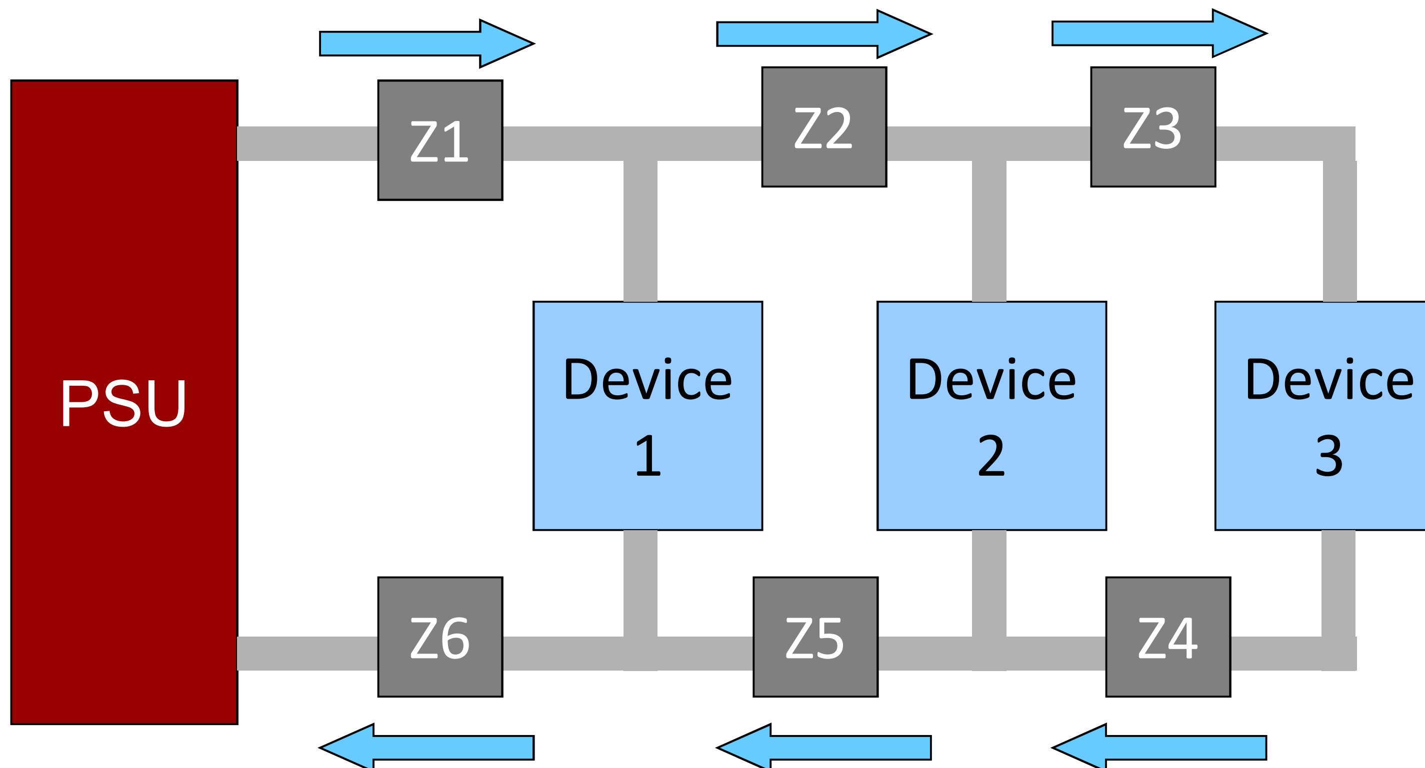

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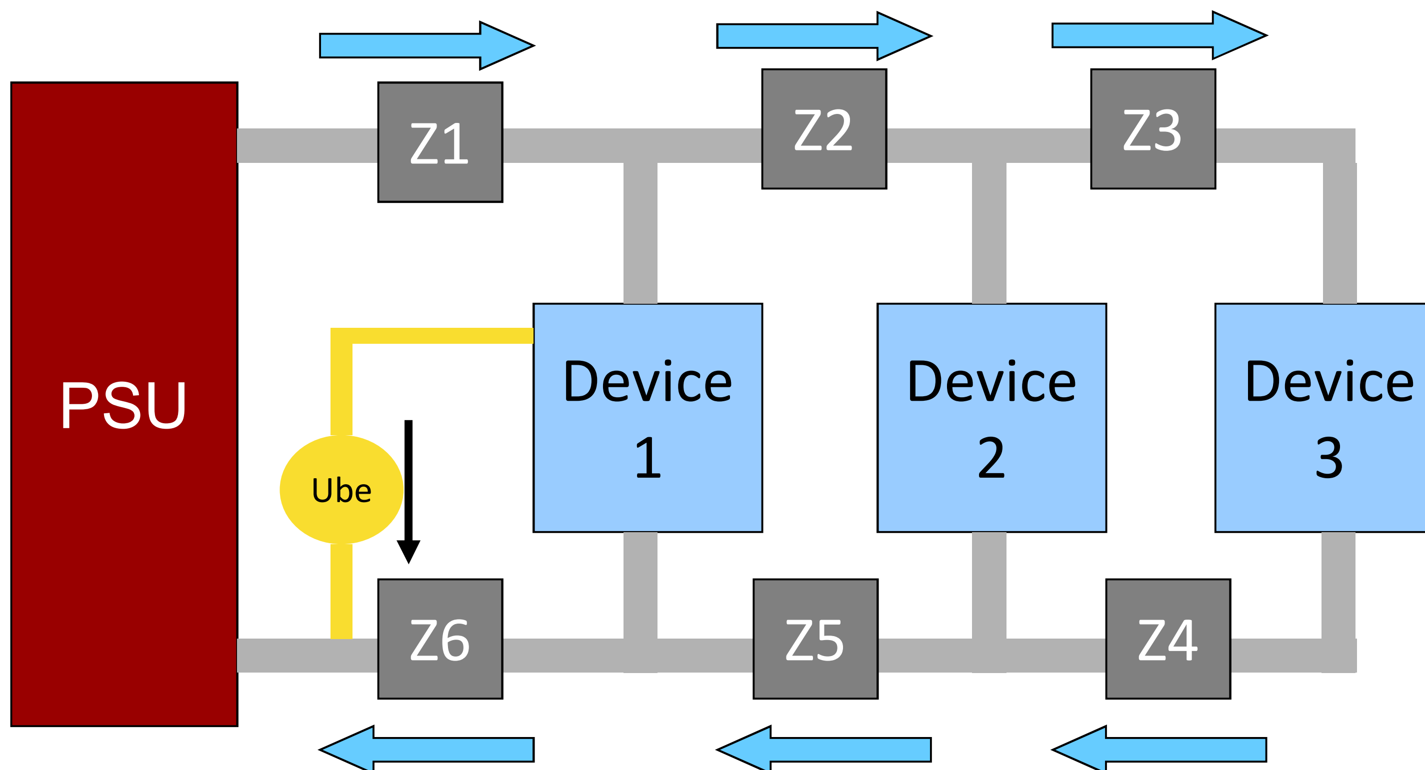
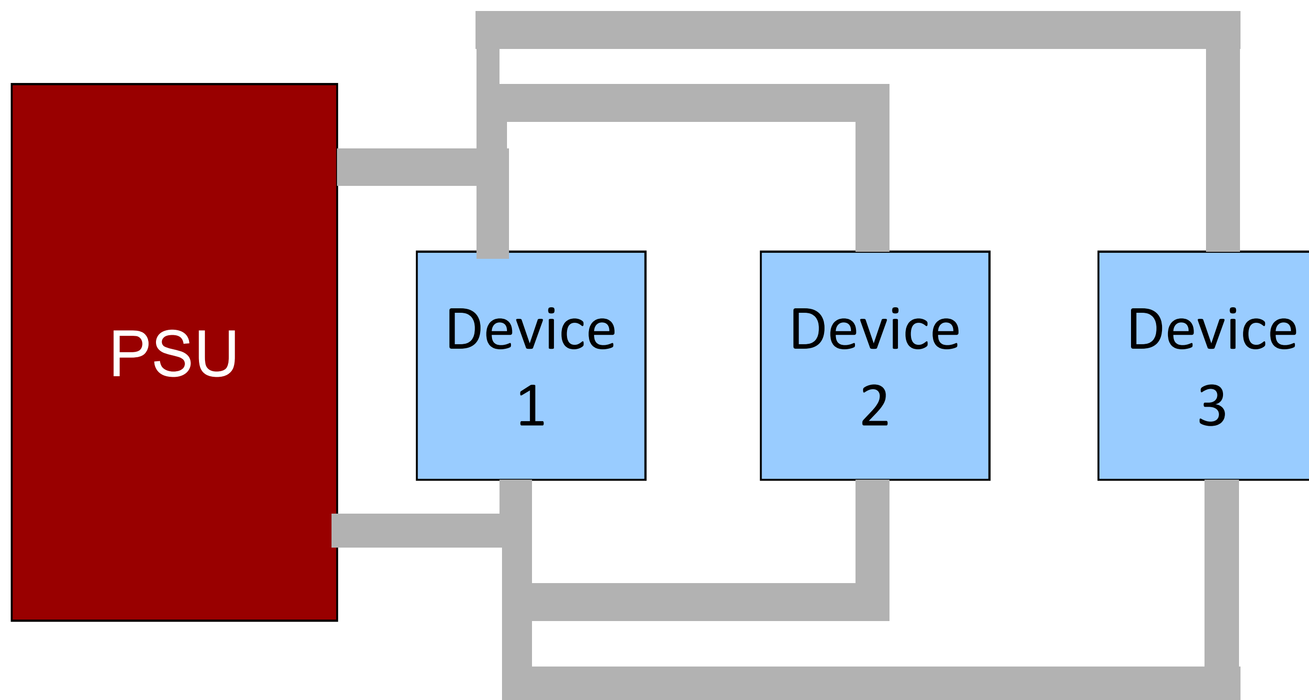


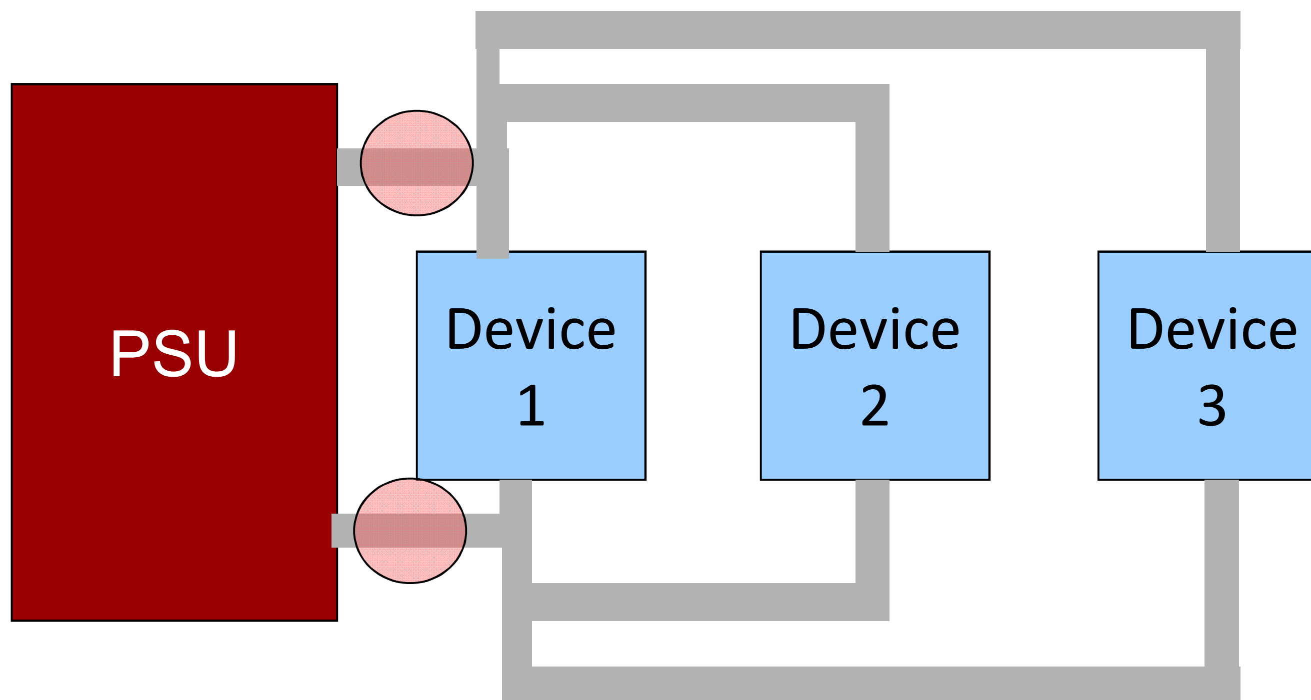
Power supply architectures
Star point

- Much better solution, but harder to wire



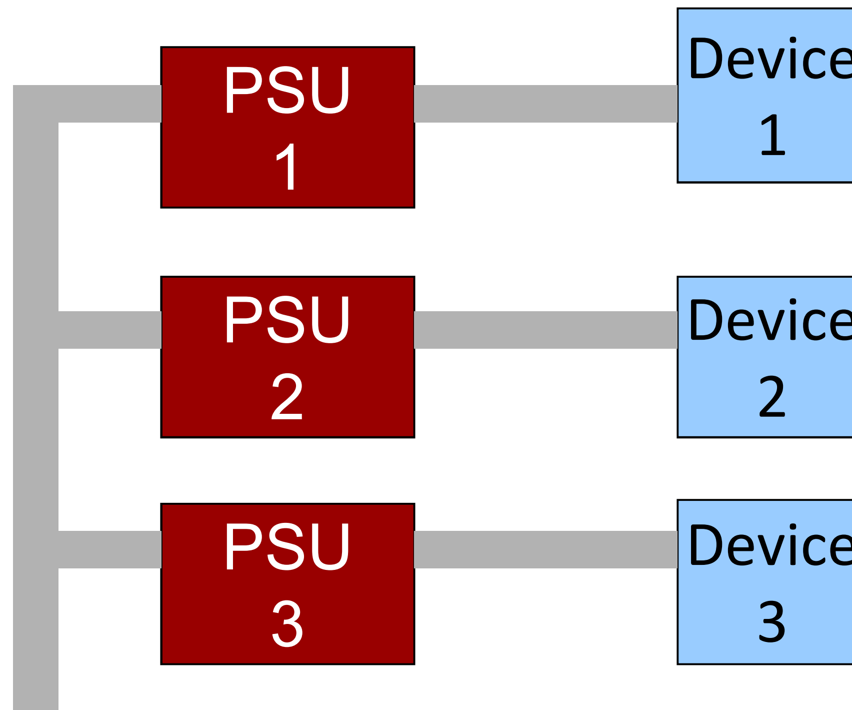
Power supply architectures
Star point

- The critical point is the common path of the star



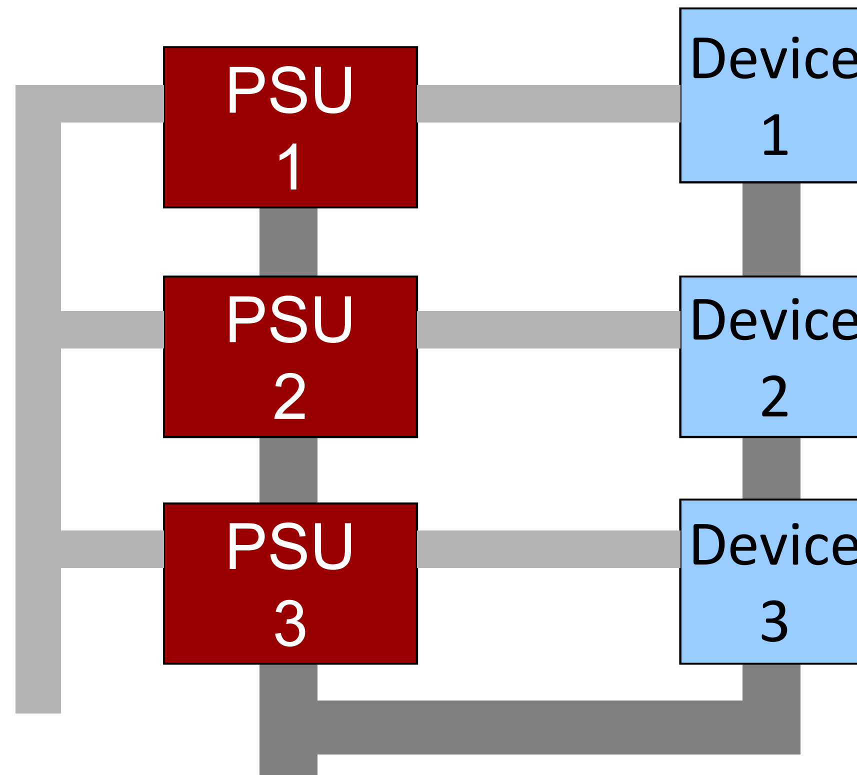
Power supply architectures
Star point with separated PSU

- Costly, but highly reduce to the common mode noises



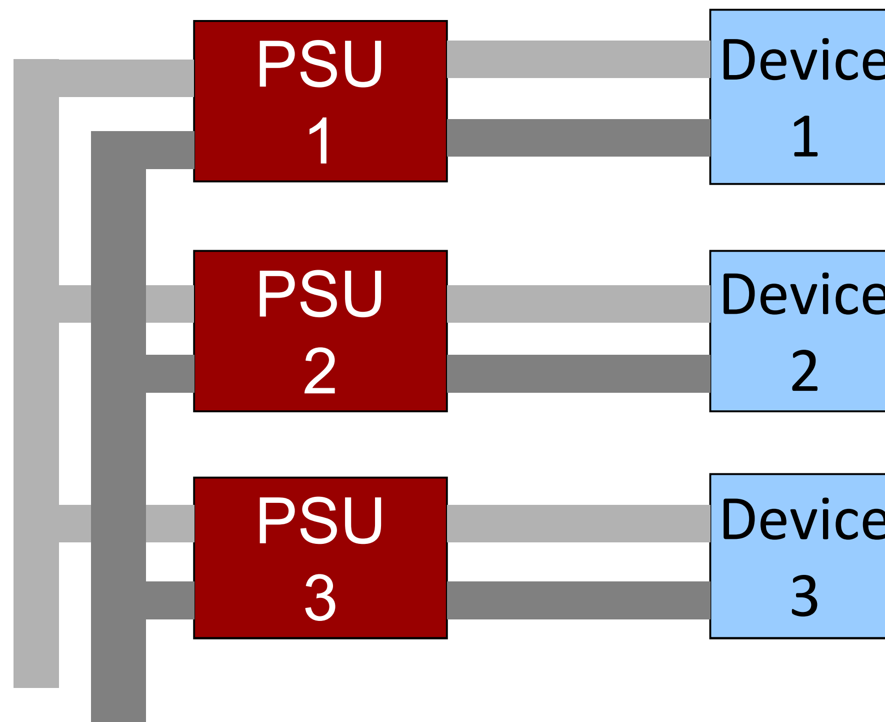
Power supply architectures
Star point with separated PSU

- Grounding can cause common impedance problems



Power supply architectures
Star point with isolated PSU

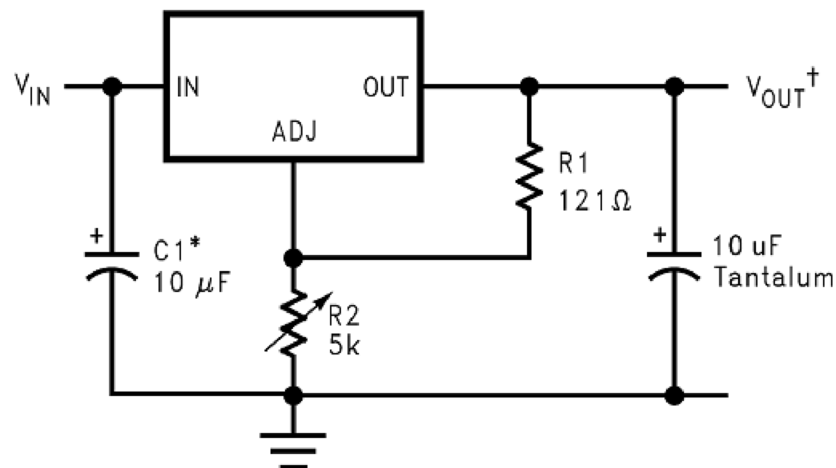
- Independent power domain
- Only differential signals can be used for communication

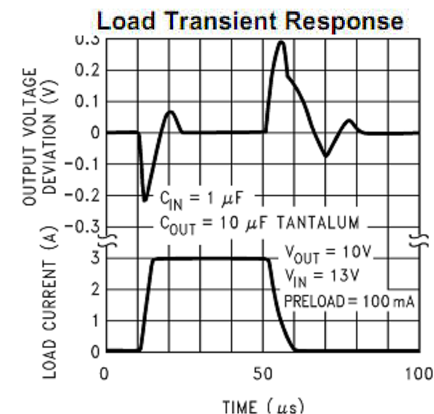


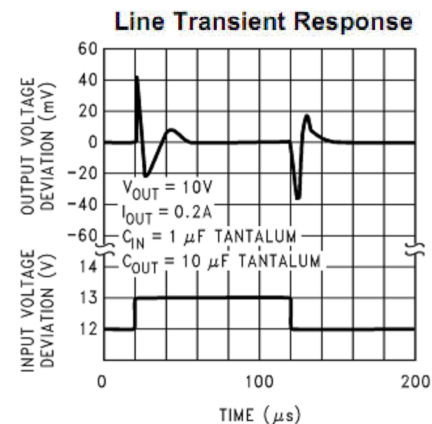
Power supply hierarchy

- There are many voltage levels needed, but it is a design decision how to create them

- Linear Voltage Regulator
  - Cheap
  - Low noise emission
  - Bad efficiency







Power supply hierarchy

- There are many voltage levels needed, but it is a design decision how to create them

- DC/DC converter
  - Costly
  - Noisy
  - Good efficiency

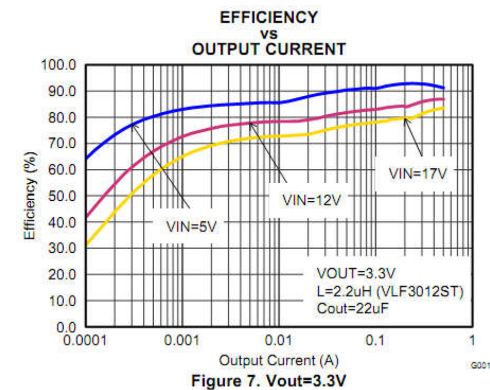
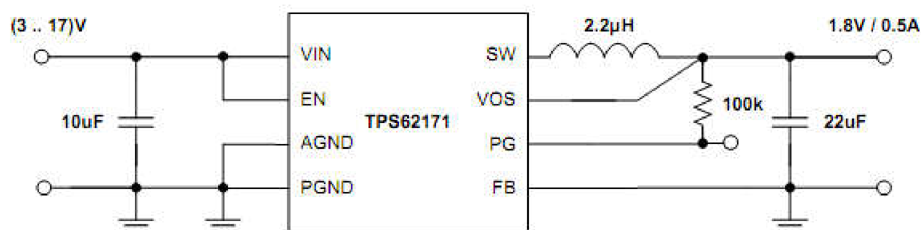


Figure 7. Vout=3.3V



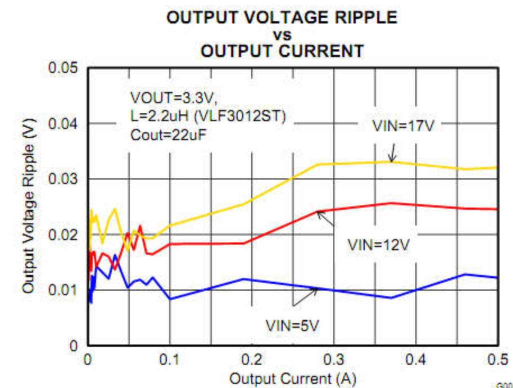
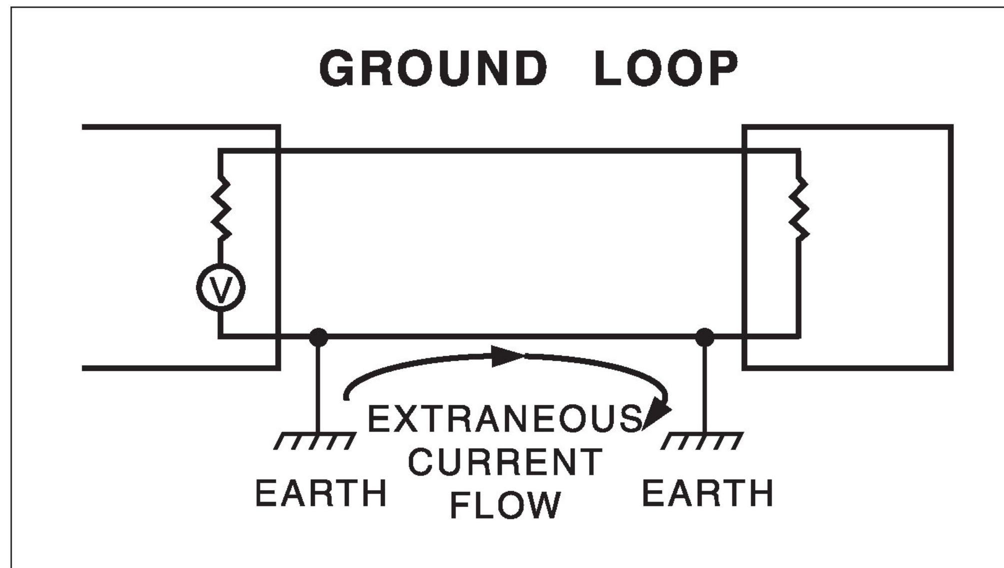


Figure 21. Output Voltage Ripple

Galvanic isolation

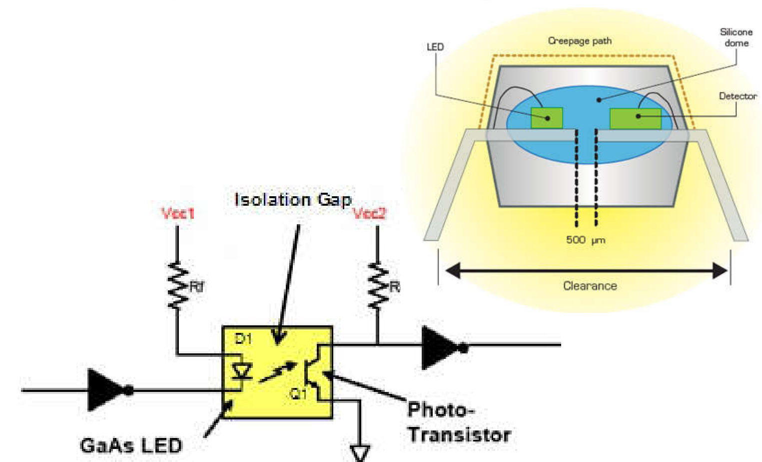
- Protecting against ground loops
- Life protection



Devices for galvanic isolation

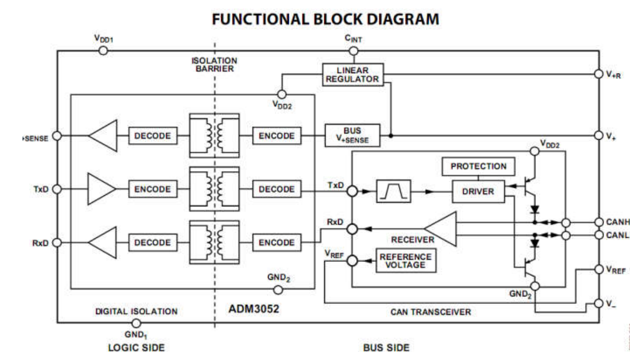
- Transformator
  - For power supply and other signal isolation

- Opto coupler
  - Fast digital communication



- Condensator
  - AC coupling

- Special purpose single chip isolators
  - CAN transciever etc.

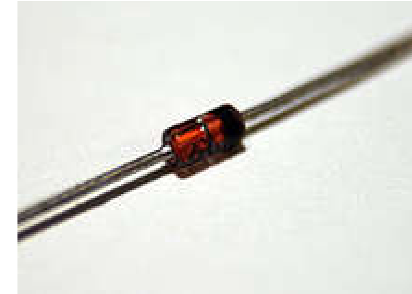


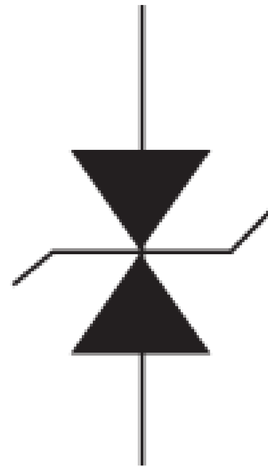
Power Supply protection

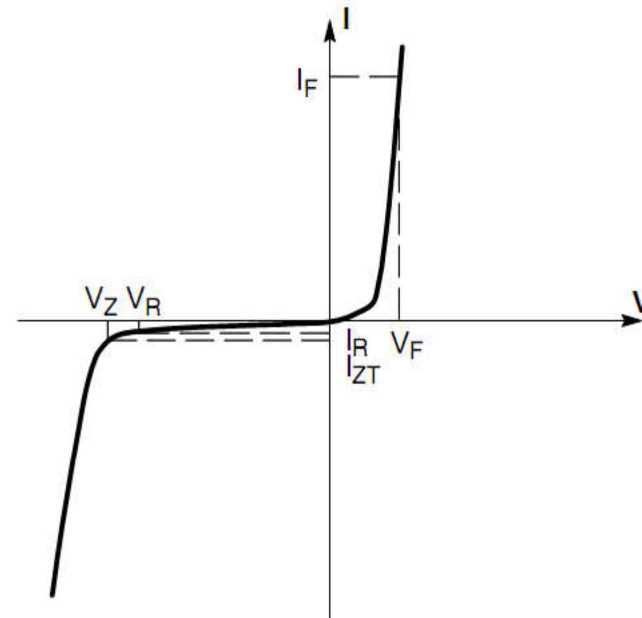
- One type of protection is nearly never enough

TVS, Zener diode

- Zener diode
  - Enery in joule
  - Operation and Zener Voltage
  - Reaction time
    - N x ns
  - Capacity

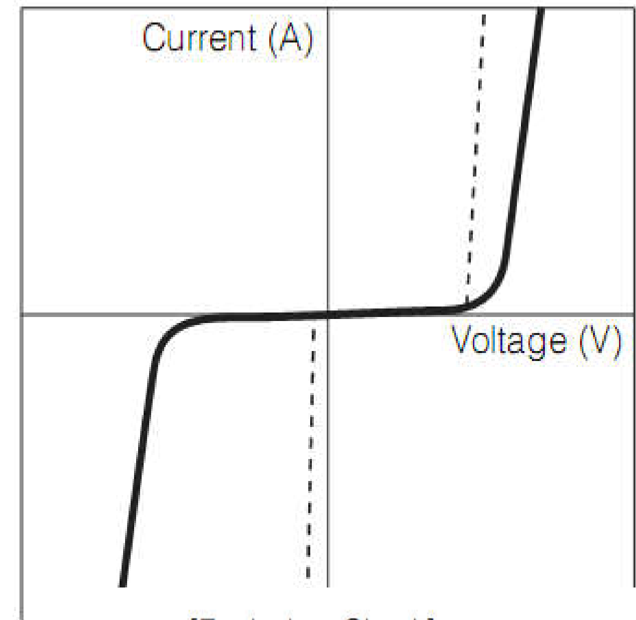


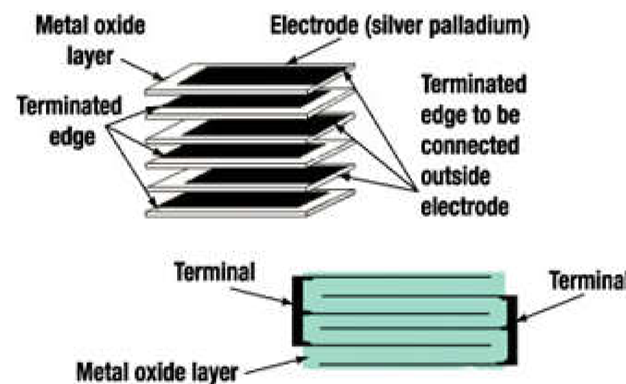


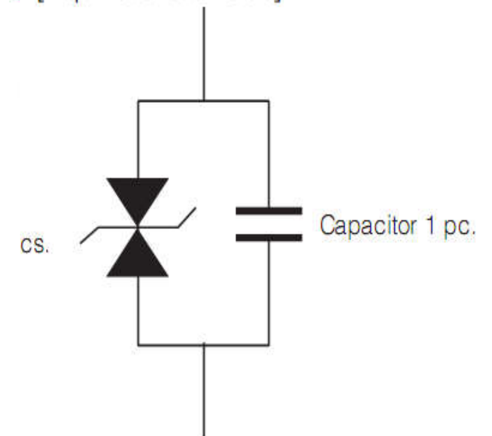


Varistor

- Variable resistor
  - Energy in joule
  - Operational Voltage
  - Reaction time
    - N*10 ns
  - Maximum current
  - Breakdown or clamping voltage
  - Energy class
    - 8/20 μs
    - 10/1000 μs
  - Passive resistance
    - N*10 Mohm

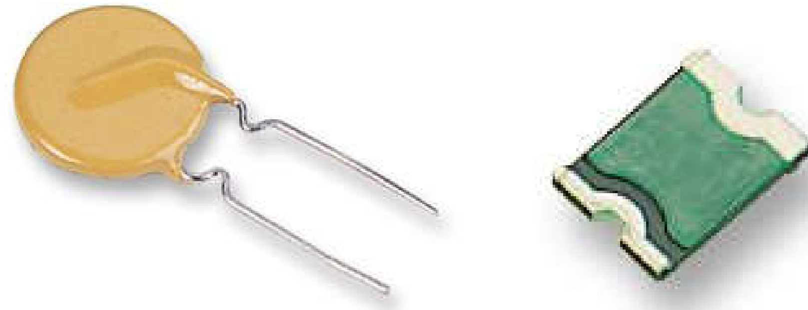


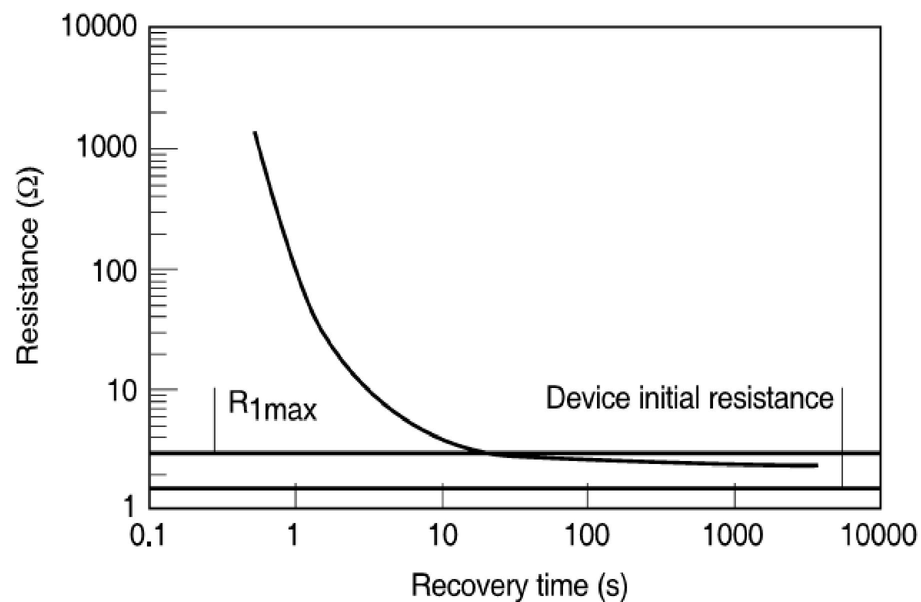


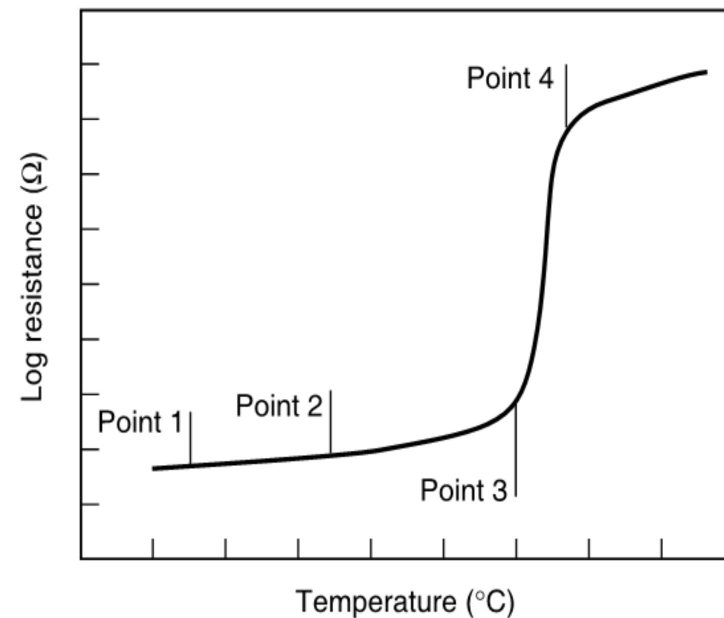


Polyswitch

- Recovering Fuse
  - Serial resistance
    - Ohm
  - Operational current
  - Breakdown current
  - Maximum current
  - Recovery time

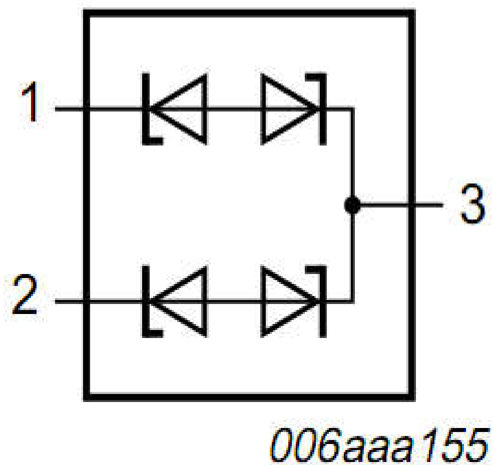


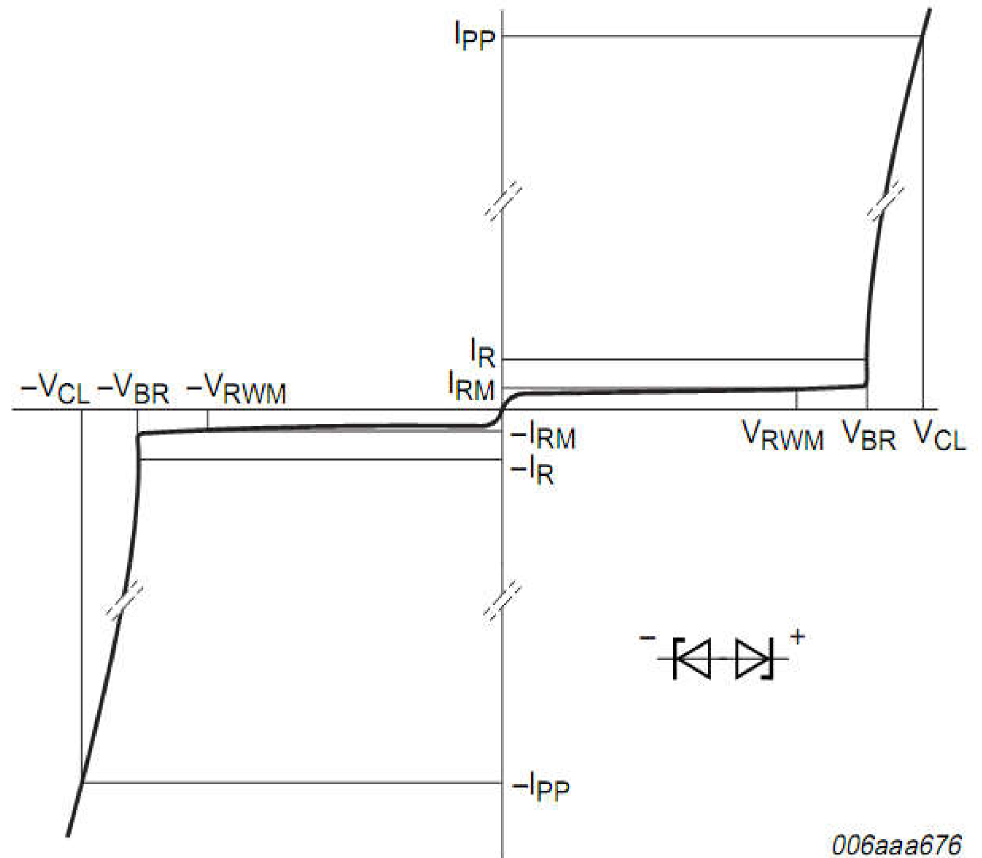




I/O pin protection

- Fast
- Cheap
- A reference voltage is needed





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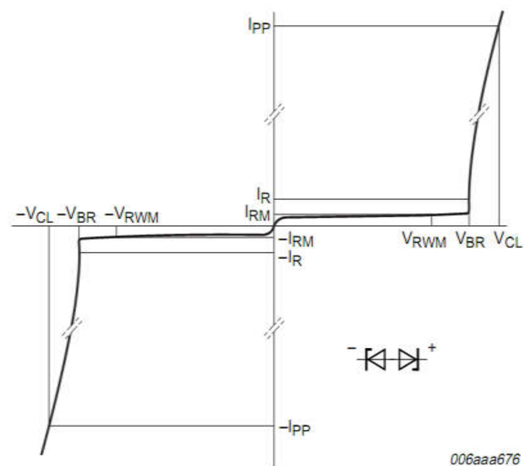
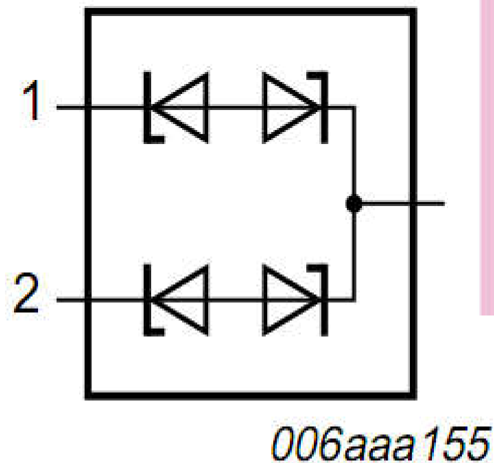
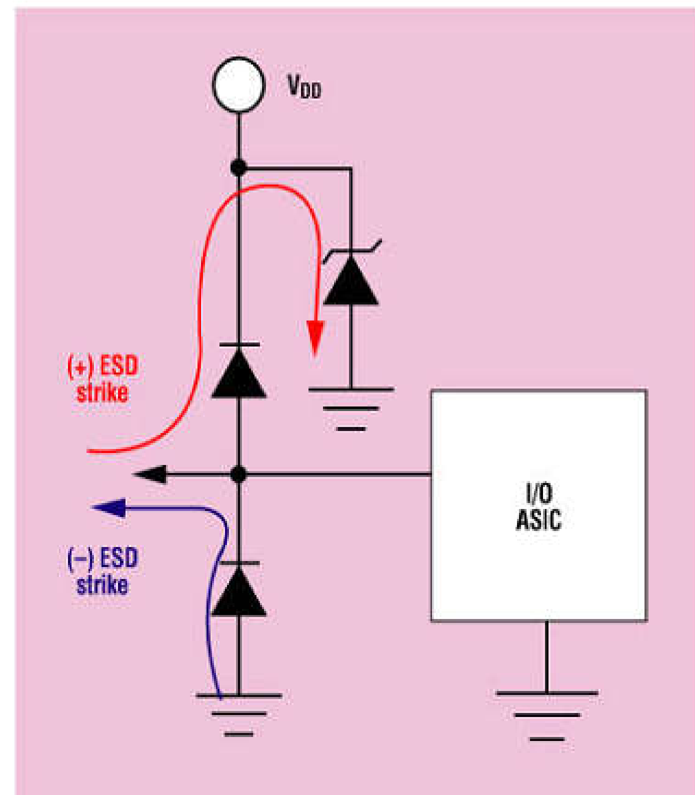
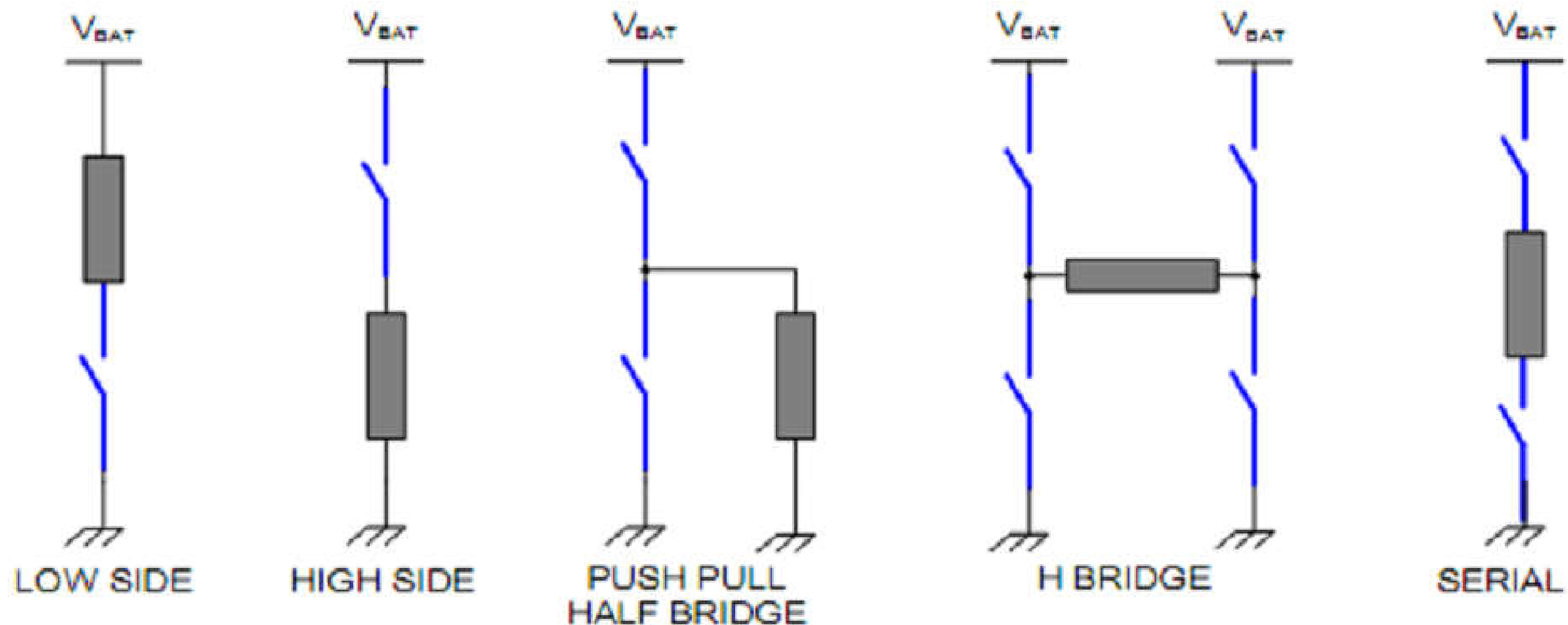




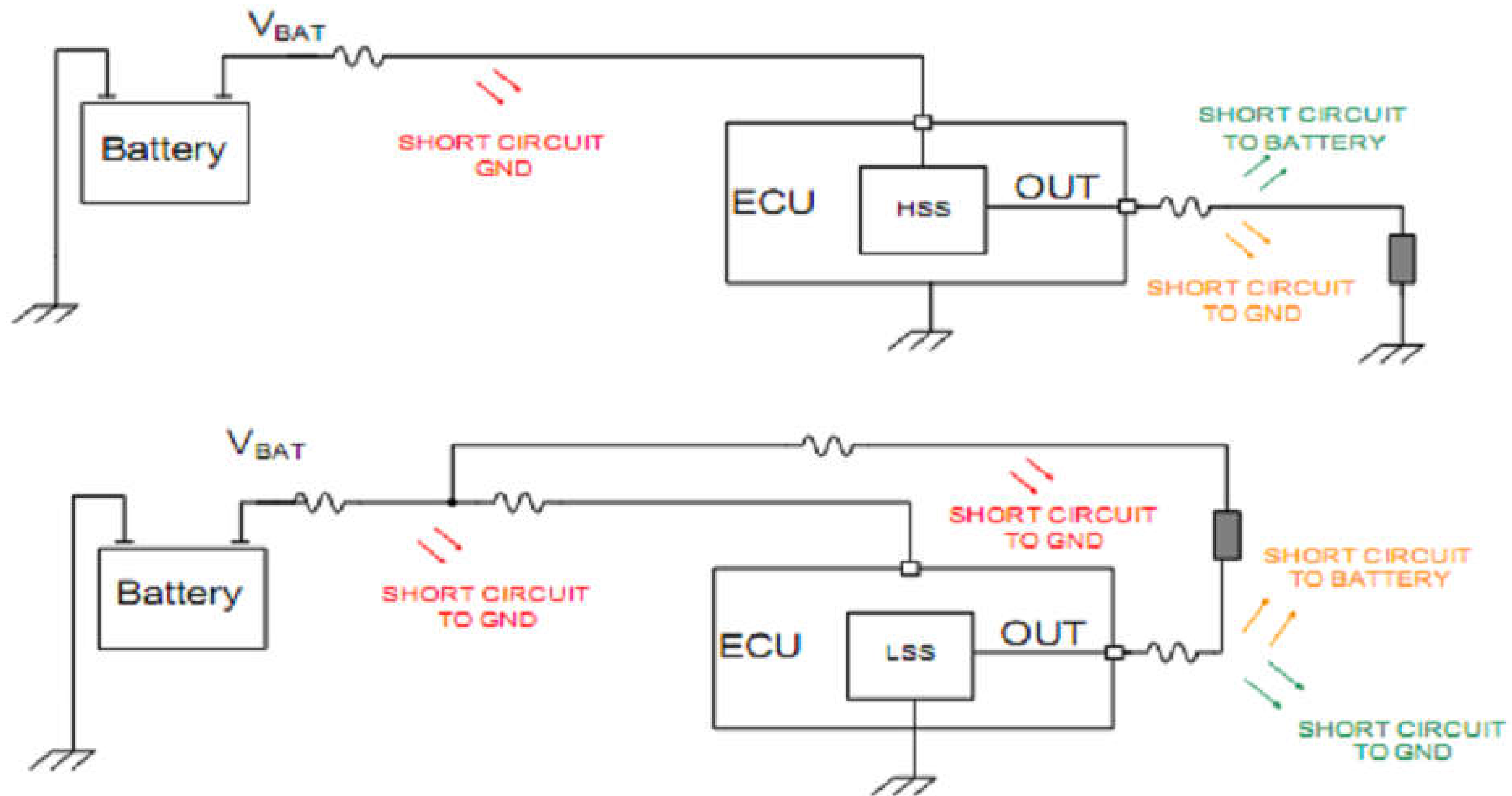


Output load switching architectures

- Typical switching architectures



High side vs Low side



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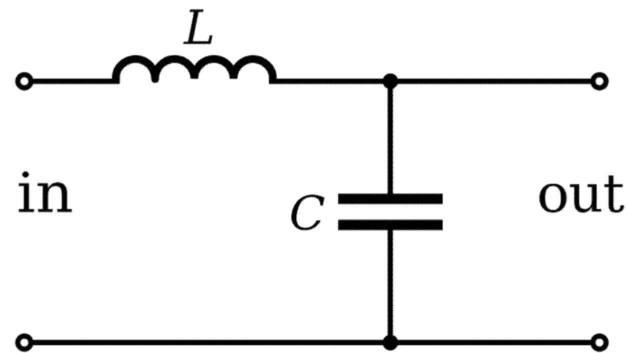
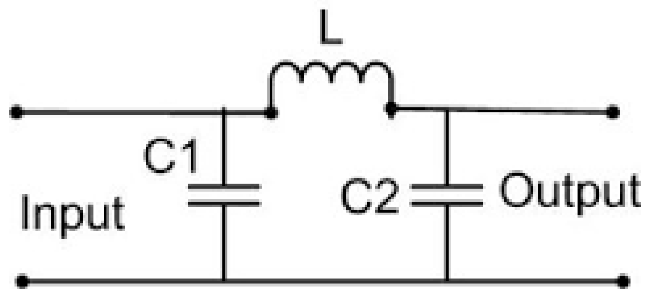
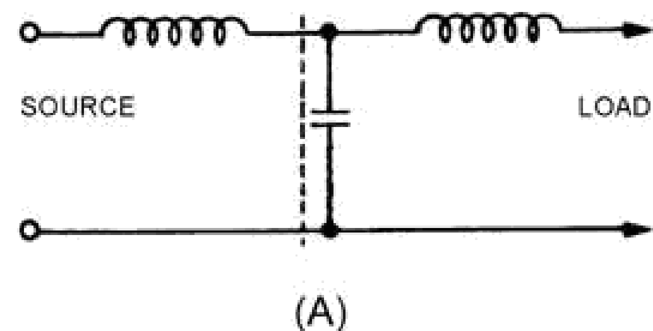
Power line filtering

- Capacitive filtering
- LC filtering
- Π or T filter
- Power supply filter

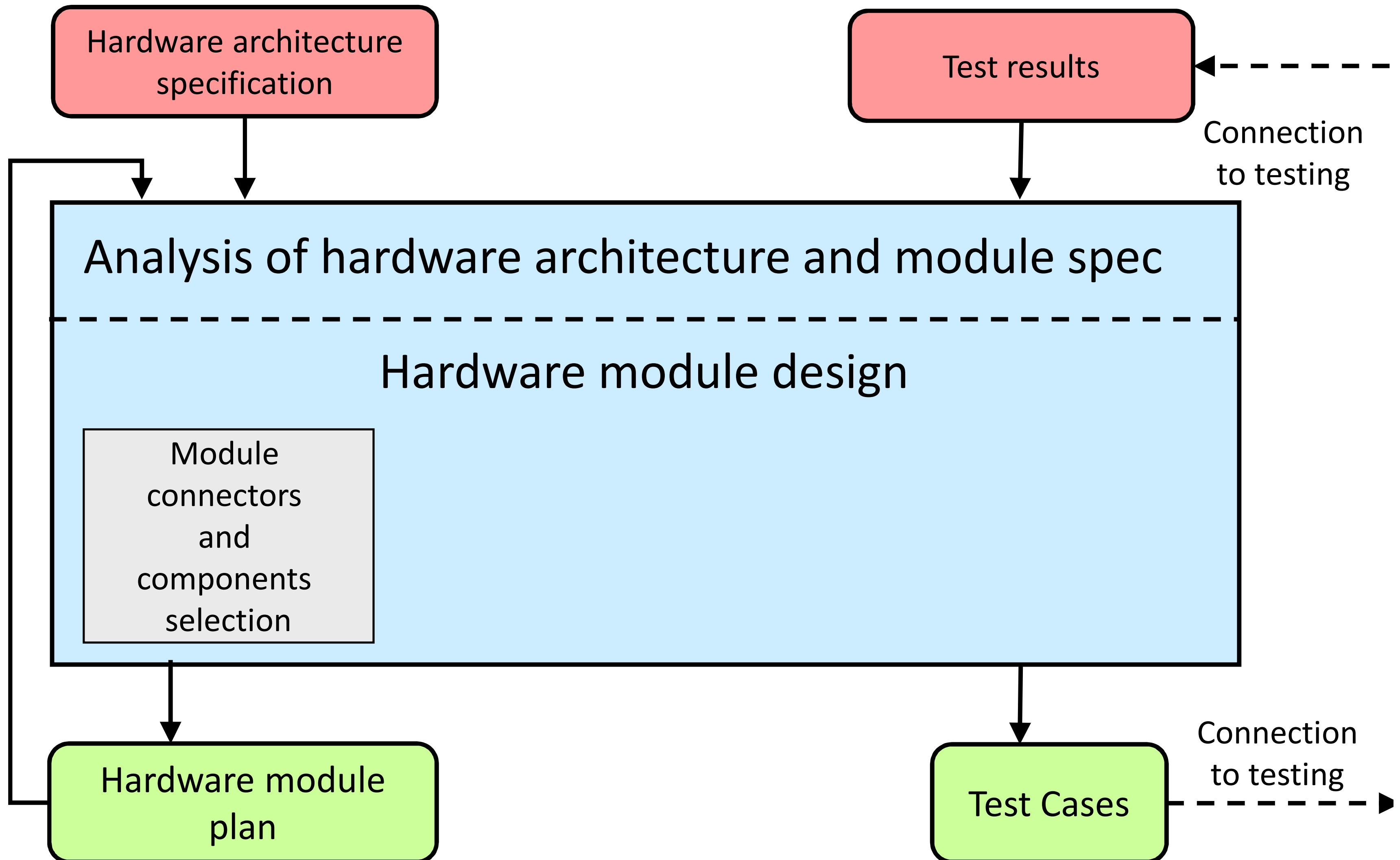






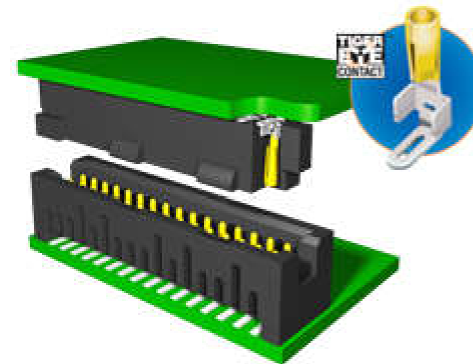
Hardware module design

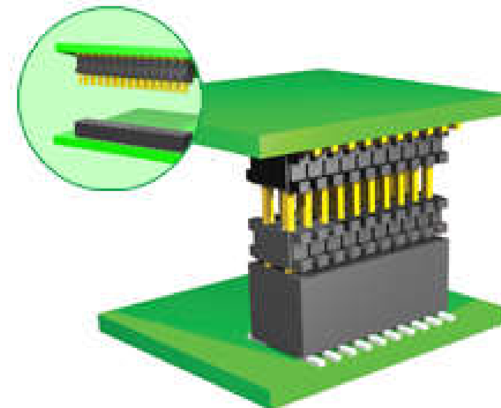
Hardware module design



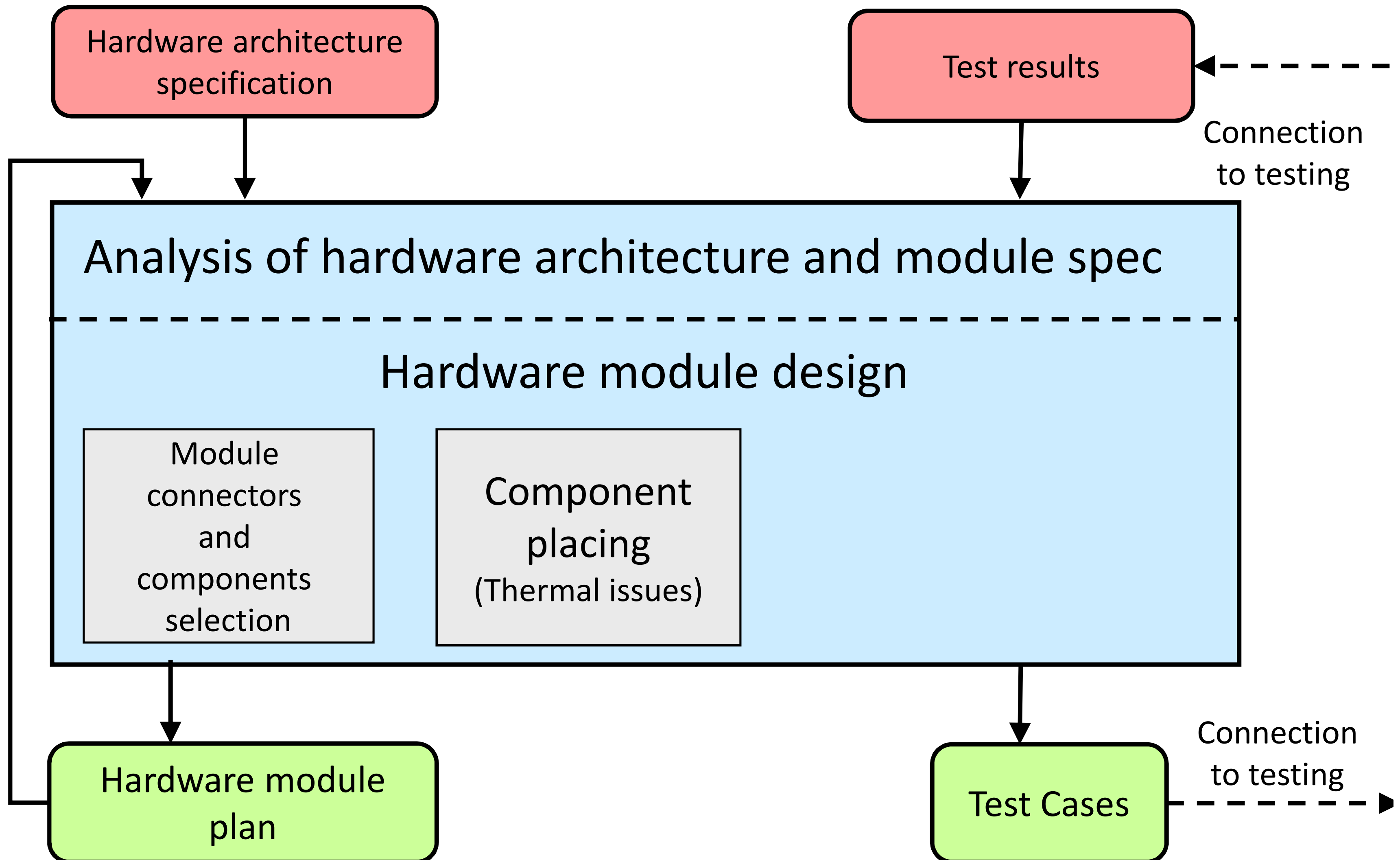
Board – to Board connectors

- Size and number of connection points
  - Voltage rating
  - Power rating
- Type of connection material
  - Current limit and impedance
  - Thin, or gold
- Mechanical stability
  - Insertion force





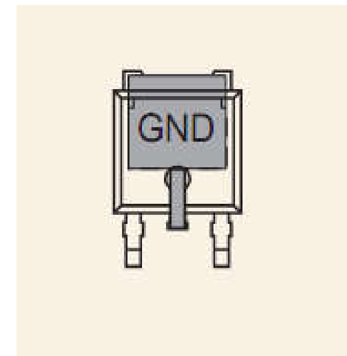
Hardware module design

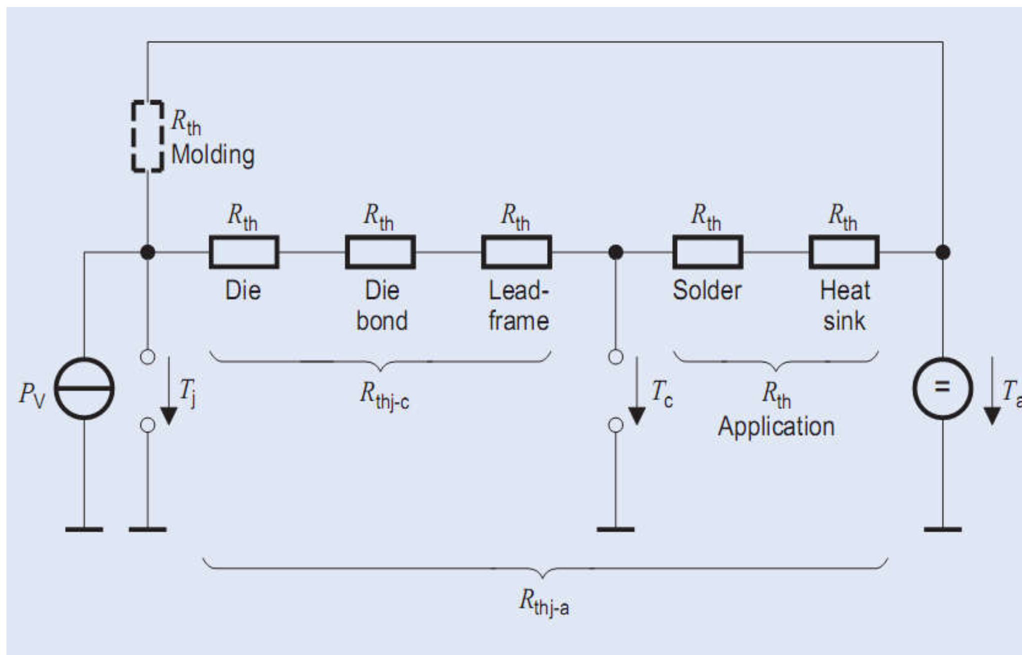


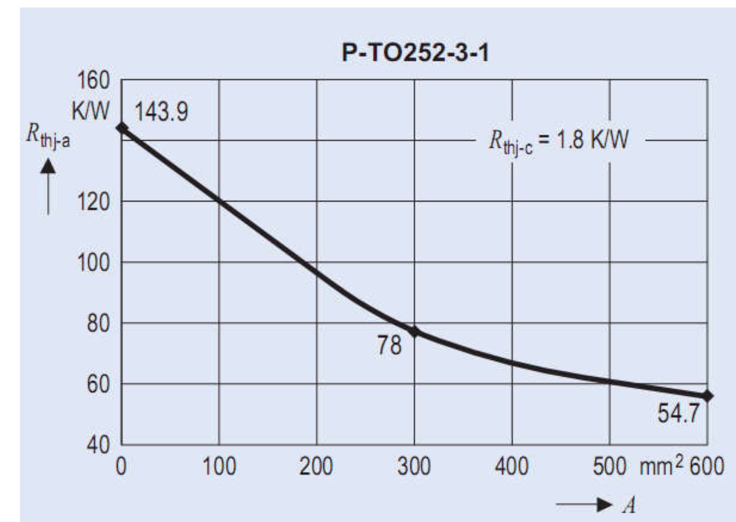
Component placing

- Make easier or harder the PCB wiring
- Must cant with the thermal properties too

$$T_{junction} = T_{ambient} + R_{thermal}(j\text{-}a) * P$$







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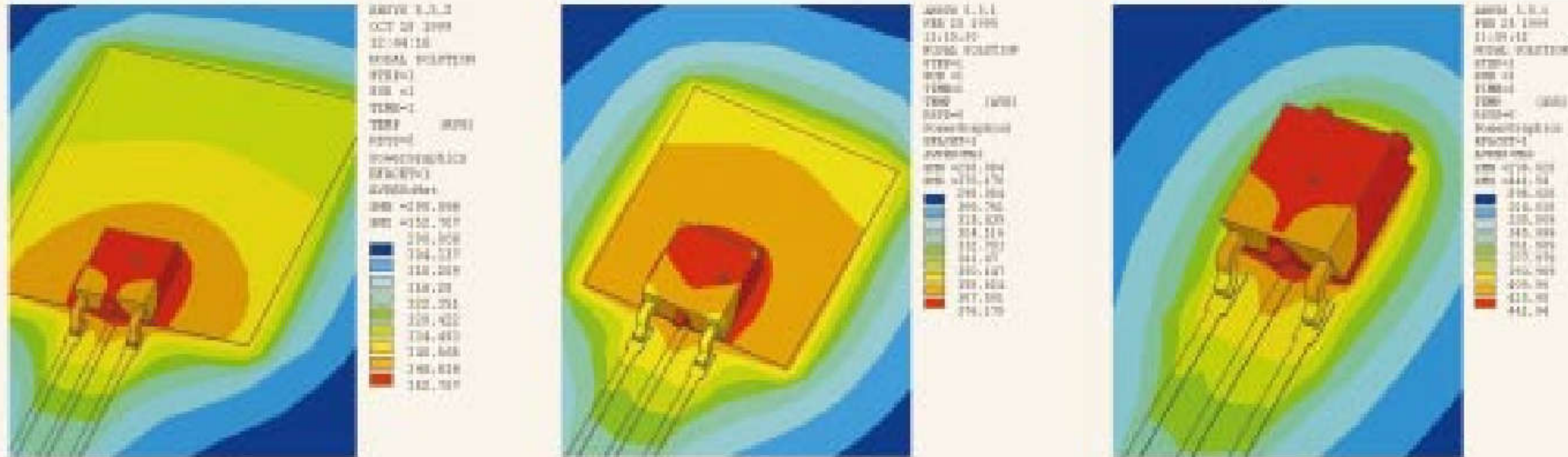
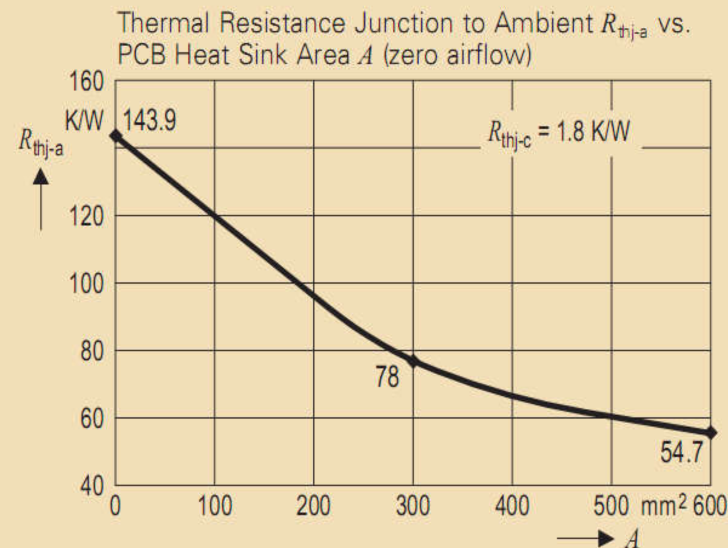
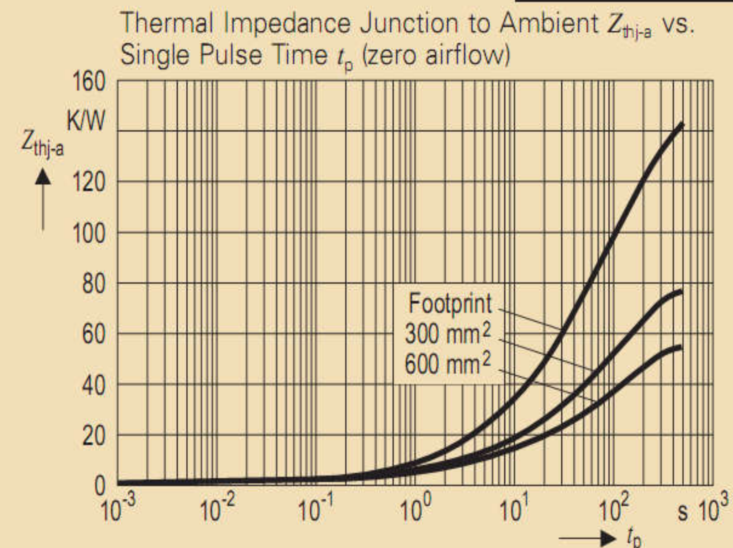
Example for thermal conducting

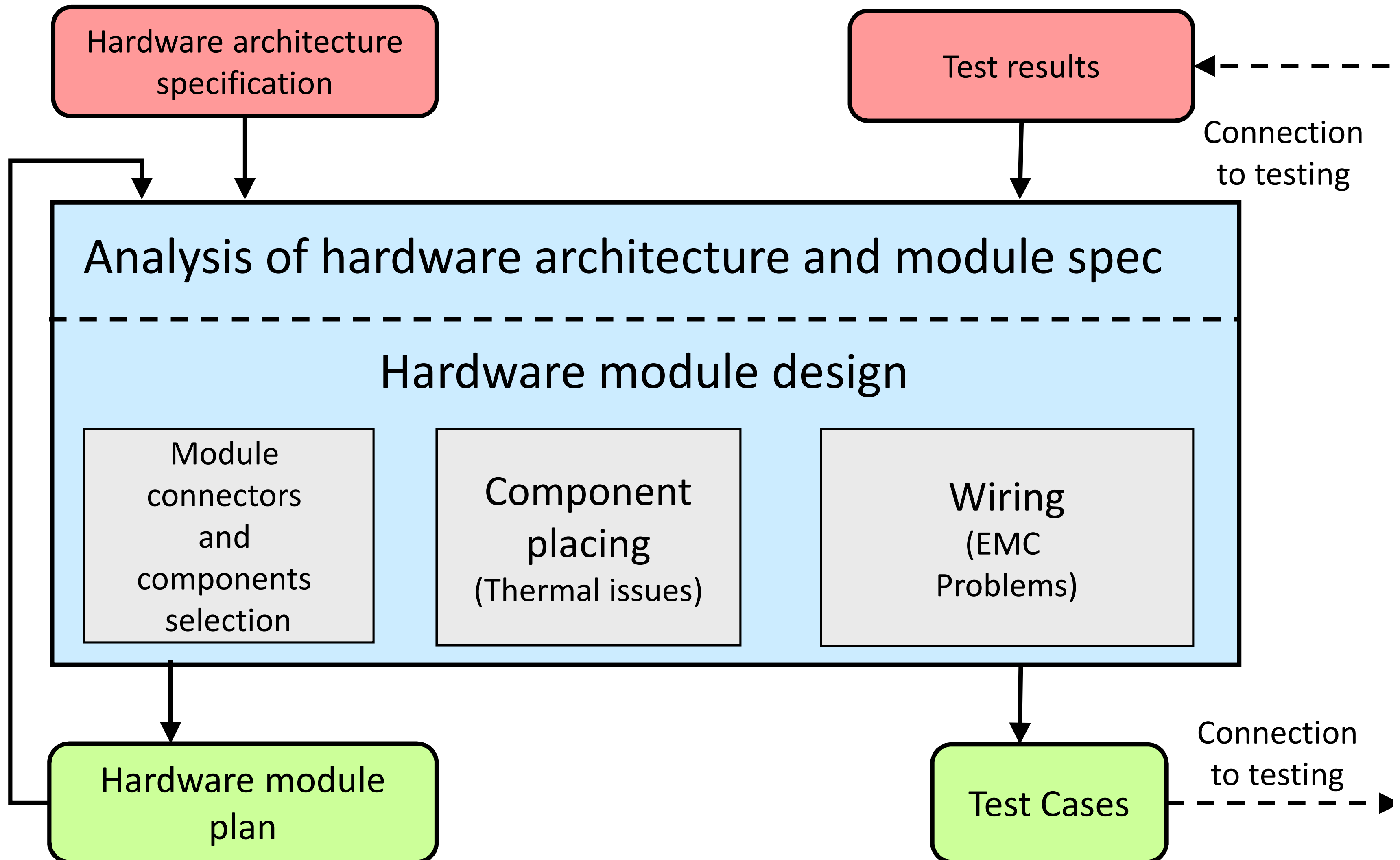


Diagrams





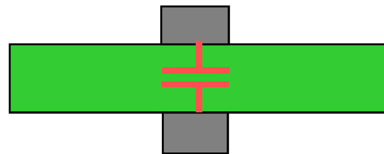
Hardware module design

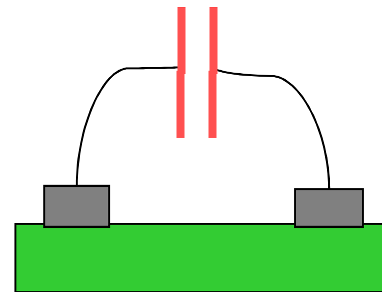


Wiring problems (EMC)

- Capacitive coupling
  - Very easy to create such during wiring

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$





  - Example: Two wire with the width of0.5mm (20mil) in a 5cm path with the distance of 3mm means: ~ 0,5 - 1 pF (ADC input impedance is ~10pF)

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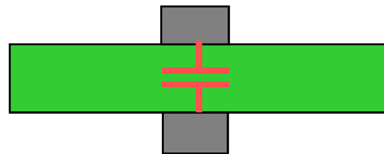
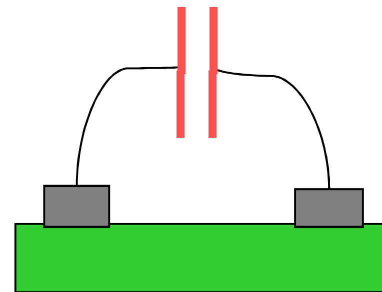


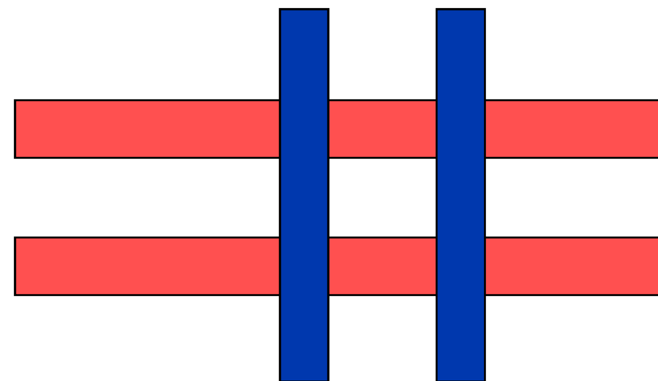


  - Example: Two wire with the width of0.5mm (20mil) in a 5cm path with the distance of 3mm means: ~ 0,5 - 1 pF (ADC input impedance is ~10pF) I'm cheating we never measure like this!!!

Wiring problems (EMC)

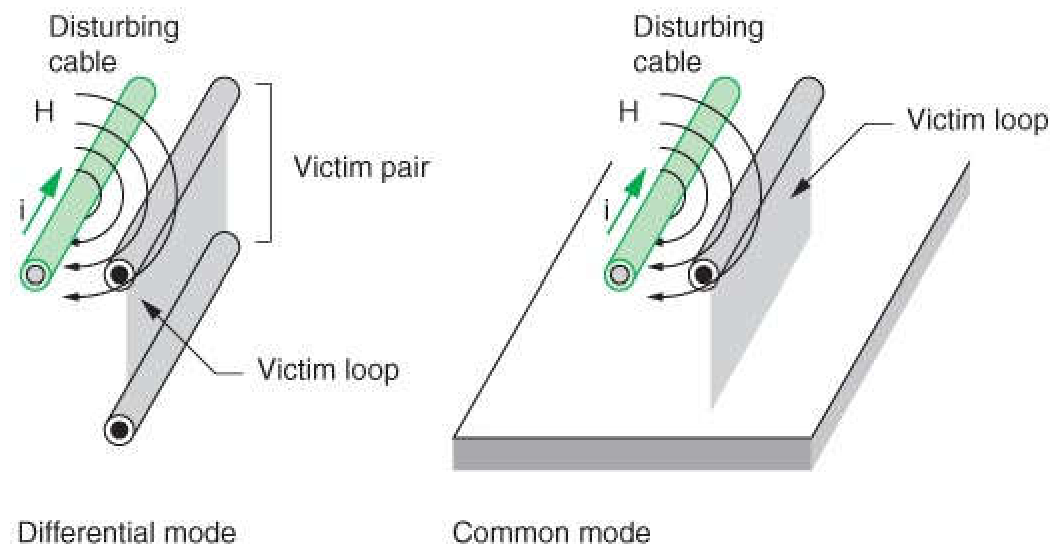
- Protecting against capacitive coupling
  - Grounding

  - With good wiring strategy



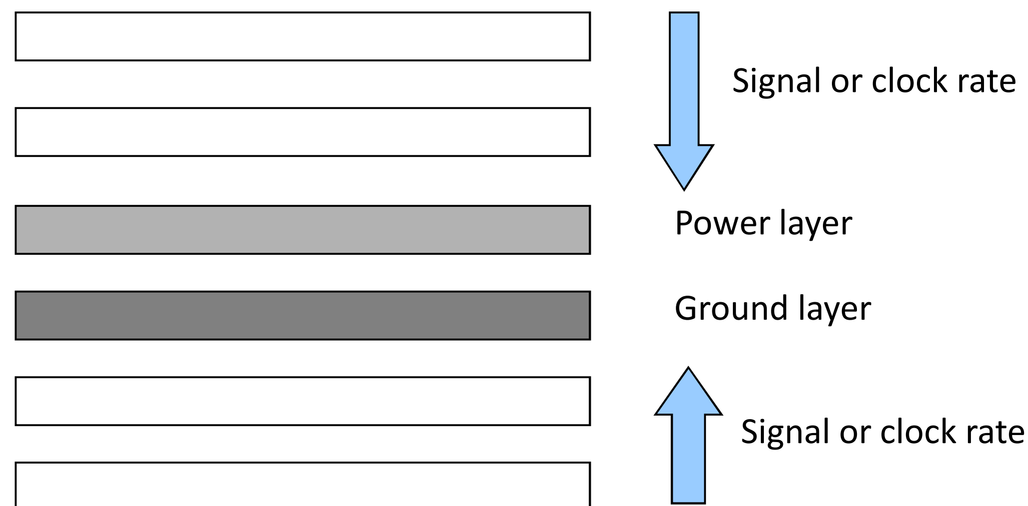
Wiring problems (EMC)

- Inductive coupling
  - Protection: make the loop smaller
  - Extra attention to the wires with significant current change
    - $U = M*di/dt$



Typical PCB layers

- The price of the PCB is rise significally with the number of layers
  - Place more then one ground layer if it is needed
  - Layer above each other should be wired perpendicular



Recommended book

- EMC for Product Designers, Fourth Edition 4th Edition
  - Tim Williams
  - ~500 pages