Lecture 1

Introduction Zynq

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Zynq PS vs. PL
Data Buses

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Zynq: A Programmable SoC

- Zynq-7000 family is an APSoC from Xilinx
- Complete ARM-based processing system
  - application processor unit (APU)
  - fully integrated memory controllers
  - I/O peripherals
- Tightly integrated programming logic
  - used to extend the processing system
  - scalable density and performance
- Flexible array of I/O
  - wide range of external multi-standard I/O
  - high-performance integrated serial transceivers
  - analog-to-digital converter inputs

The slides are based on Xilinx Tutorials.

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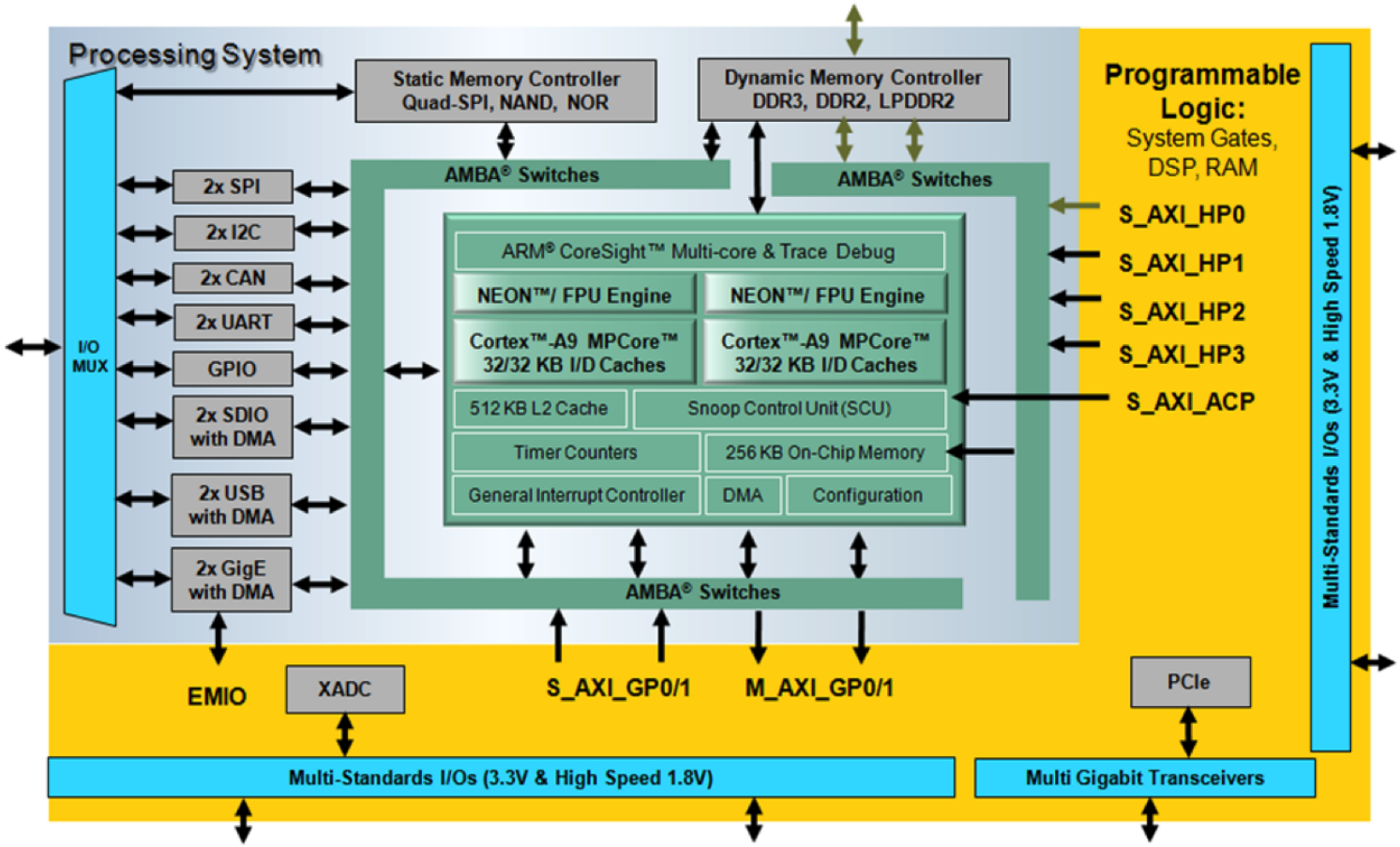
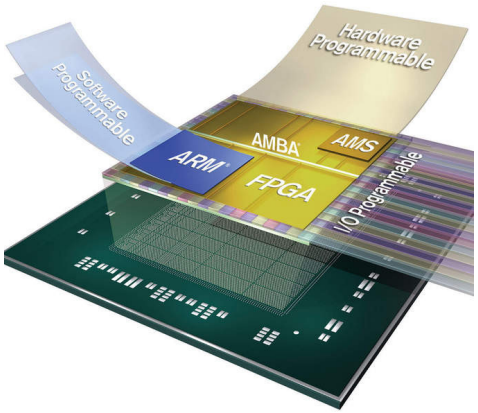
Zynq SoC Block Diagram



Processor and Hardware Logic

- The Zynq-7000 SoC architecture consists of two major sections:
- PS: processing system
  - dual ARM Cortex-A9 processors, 866MHz to 1GHz frequency
  - multiple peripherals
  - hard silicon core
- PL: programmable logic
  - shares the same FPGA series 7 programmable logic
  - logic cells: 28k - 444k (430k to 6.6M gates)
  - flip-flops: 35k - 554k
  - DSP/MAC: 80 - 2020
  - peak DSP performance: 100 - 2622 GMACs
  - AD converter: two 12bits

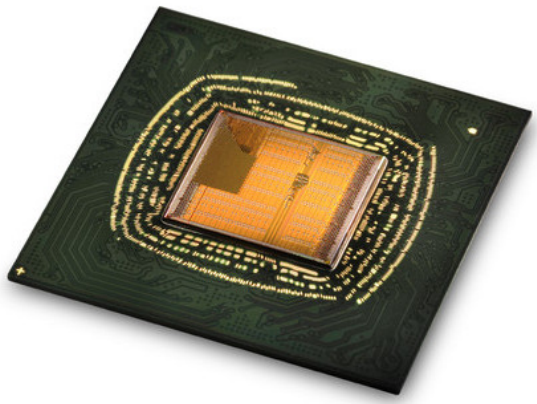


ARM Processor Architecture

- ARM Cortex-A9 processor implements the ARMv7-A architecture
  - ARMv7 is the ARM instruction set architecture ISA
  - ARMv7-A: application set that includes support for a MMU
  - ARMv7-R: real-time set that includes support for a memory protection unit MPU
  - ARMv7-M: microcontroller set that is the smallest set
- ARMv7 ISA includes the following types of instructions (for backward compatibility)
  - Thumb instructions: 16 bits, Thumb-2 instructions: 32 bits
  - NEON: ARMs single instruction multiple data instructions
- ARM advanced microcontroller bus architecture (AMBA) protocol
  - AXI3: third-generation ARM interface
  - AXI4: adding to existing AXI definitions (extended bursts, subsets)
- Cortex is the new family of processors

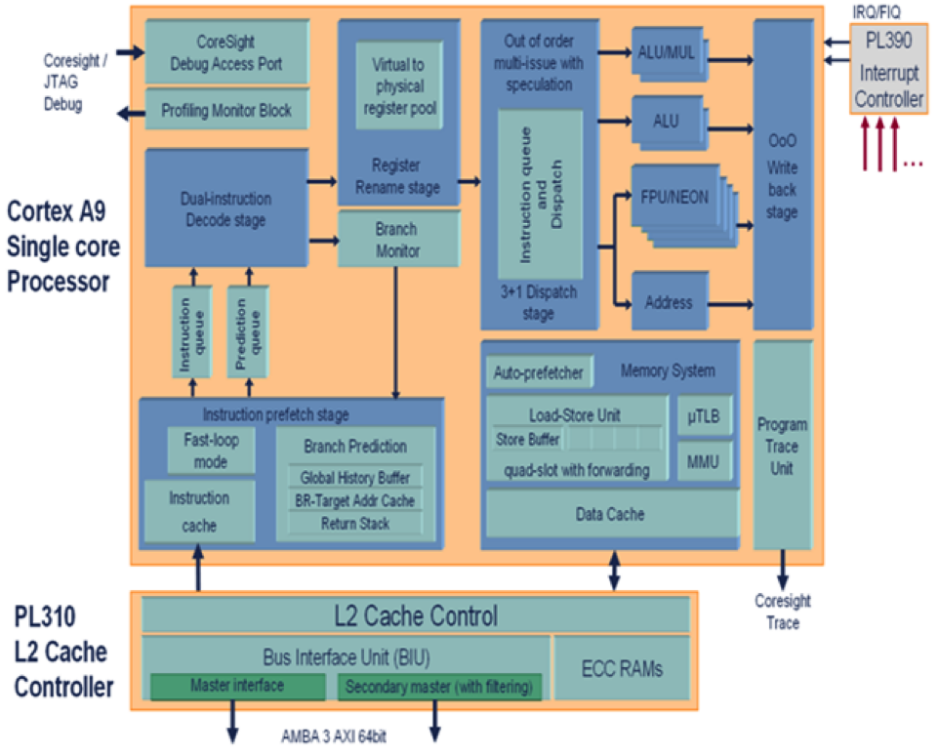
ARM Cortex-A9 Processor Power

- dual-core processor cluster
- 2.5 DMIP/MHz per processor
- Harvard architecture
- self-contained 32KB L1 caches for instruction and data
- external memory based 512KB L2 cache
- automatic cache coherencey between processor cores
- 1 GHz operation (fastest speed grade)



Cortex-A9 Processor Micro-Architecture (1)

- instruction pipeline supports out-of-order instruction issue and completion
- register renaming to enable execution speculation
- non-blocking memory system with load-store forwarding
- fast loop mode in instruction pre-fetch to low power consumption



Cortex-A9 Processor Micro-Architecture (2)

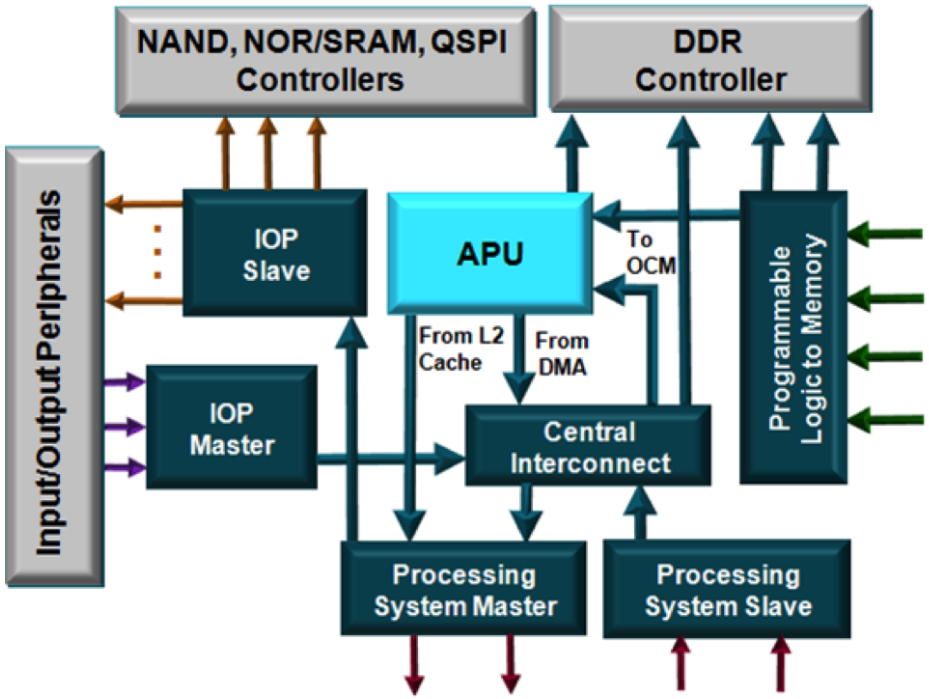
- variable length, out-of-order, eigth-stage, super-scalar instruction pipeline
  - advanced pre-fetch with parallel branch pipeline enabling earlier branch prediction and resolution
- speculative execution
  - supports virtual renaming of ARM physical registers to remove pipeline stall due to data dependencies
  - increased processor utilization and hiding of memory latencies
  - increased performance by hardware unrolling of code loops
  - reduced interrupt latency via speculative entry to Interrupt Service Routine ISR

Processor System Components

- application processing unit (APU)
- I/O peripherals (IOP)
  - multiplexed I/O (MIO), extended multiplexed I/O (EMIO)
- memory interfaces
- PS interconnect
- DMA
- timers
- general interrupt controller GIC
- on-chip memory (OCM): RAM
- debug controller: CoreSight

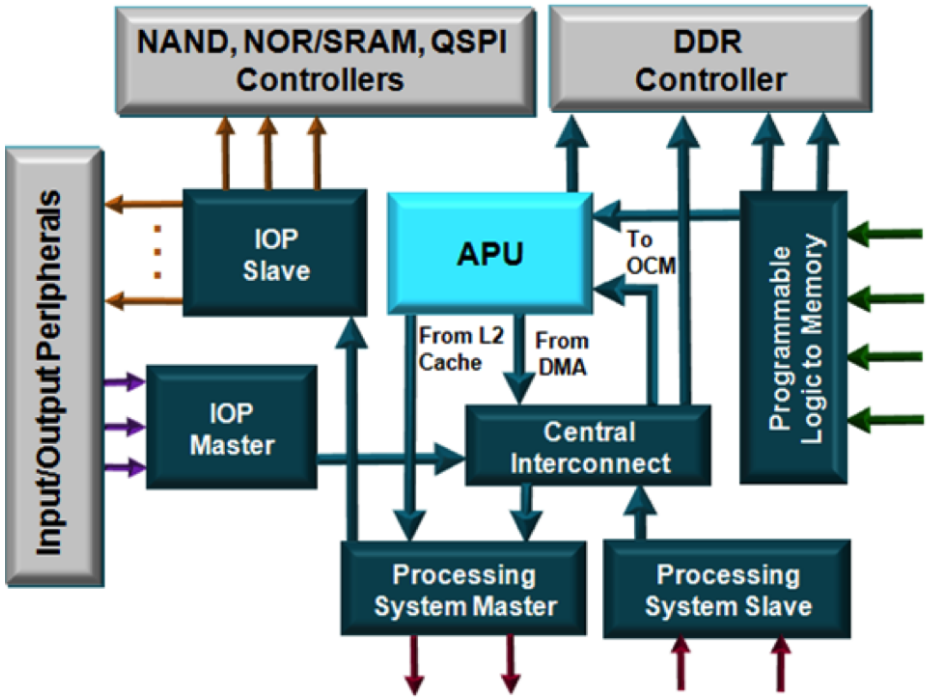
Processor System Interconnect (1)

- programmable logic to memory
  - two ports to DDR
  - one port to OCM SRAM
- central interconnect
  - enables other interconnects to communicate
- peripheral master
  - USB, GigE, SDIO connects to DDR and PL via the central interconnect
- peripheral slave
  - CPU, DMA, and PL access to IOP



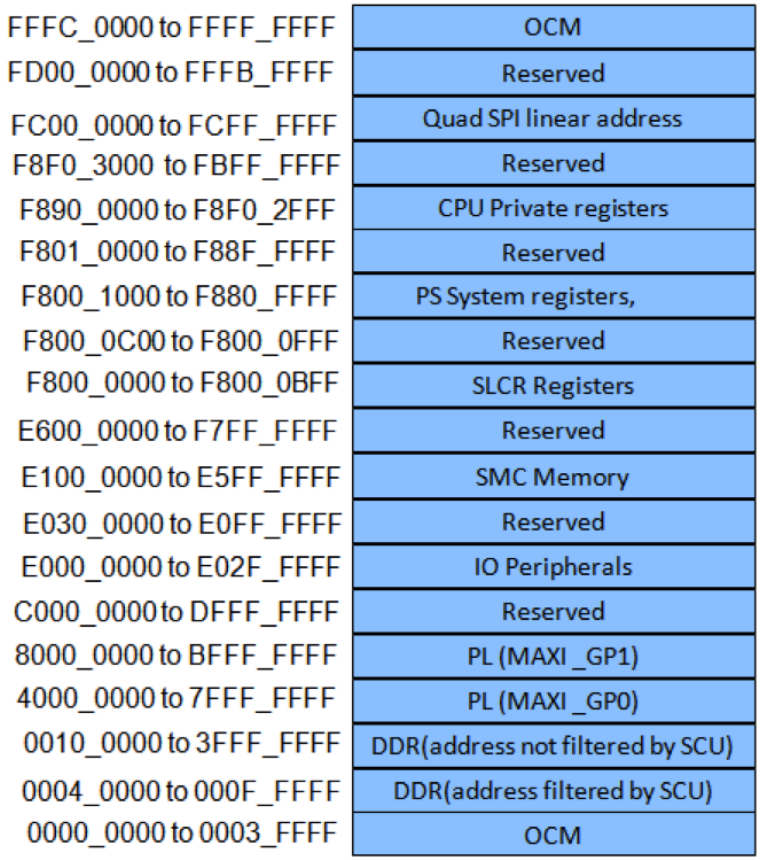
Processor System Interconnect (2)

- processing system master
  - two ports from the processing system to programmable logic
  - connects the CPU block to common peripherals through the central interconnect
- processing system slave
  - two ports from programmable logic to the processing system



Memory Map

- the Cortex-A9 processor uses 32-bit addressing
- all PS and PL peripherals are memory mapped to the Cortex-A9 processor cores
- all slave PL peripherals will be located between: 40000000 and 7FFFFFFF (connected to GP0) and 80000000 and BFFFFFFF (connected to GP1)



Memory Resources

- on-chip memory (OCM)
  - RAM
  - boot ROM
- DDRx dynamic memory controller
  - supports LPDDR2, DDR2, DDR3
- flash/static memory controller
  - supports SRAM, QSPI, NAMD/NOR flash

PS Boots First

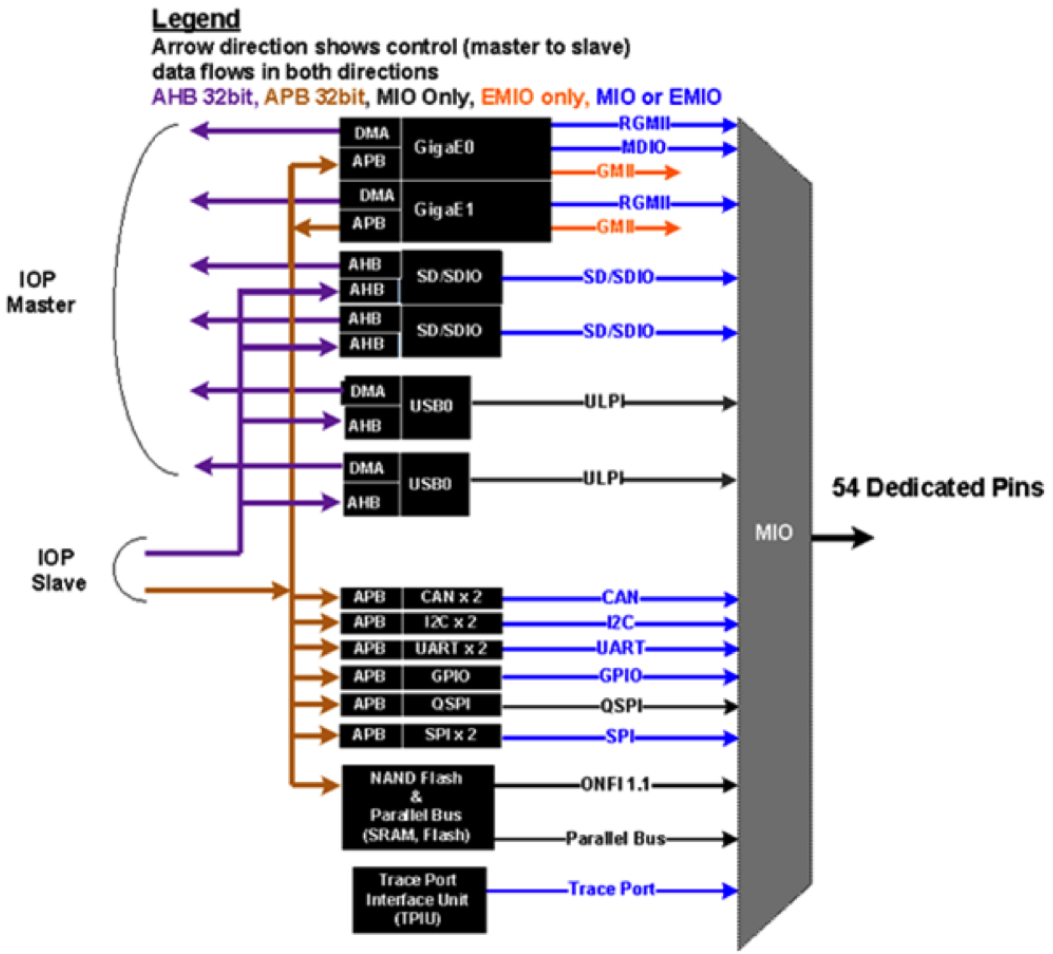
- CPU0 boots from OCM ROM; CPU1 goes into a sleep state
- on-chip boot loader in OCM ROM (stage 0 boot)
- processor loads First Stage Boot Loader (FSBL) from external flash memory
  - NOR
  - NAND
  - Quad SPI
  - SD card
  - JTAG: not a memory device - used for development/debug only
  - boot source selected via package bootstrapping pins
- optional secure boot mode allows the loading of encrypted software from the flash boot memory

Configuring the PL

- the programmable logic is configured after the PS boots
- performed by application software which is accessing the hardware device configuration unit
  - bitstream image transfered
  - 100MHz, 32-bit PCAP stream interface
  - decryption/authentication hardware option for encrypted bitstream (in secure boot mode, this option can be used for software memory load)
  - built-in DMA allows simultaneous PL configuration and OS memory loading

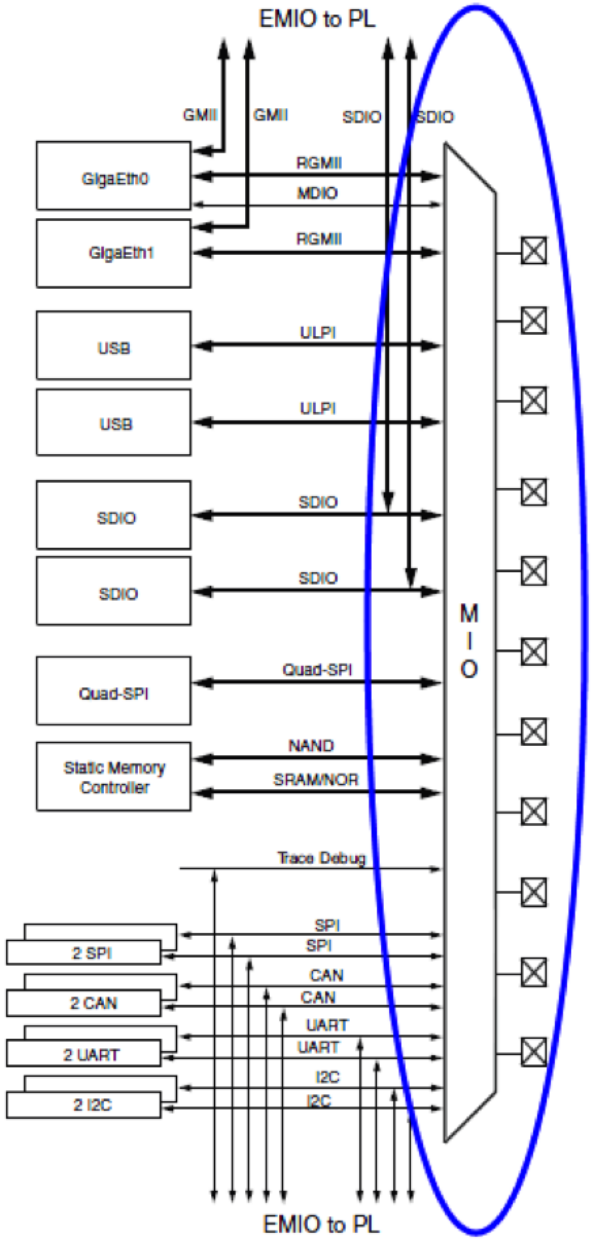
Input/Output Peripherals

- two GigE
- two USB
- two SPI
- two SD/SDIO
- two CAN
- two I2C
- two UART
- four 32-bit GPIO
- static memories
  - NAND, NOR/SRAM, QSPI
- trace ports



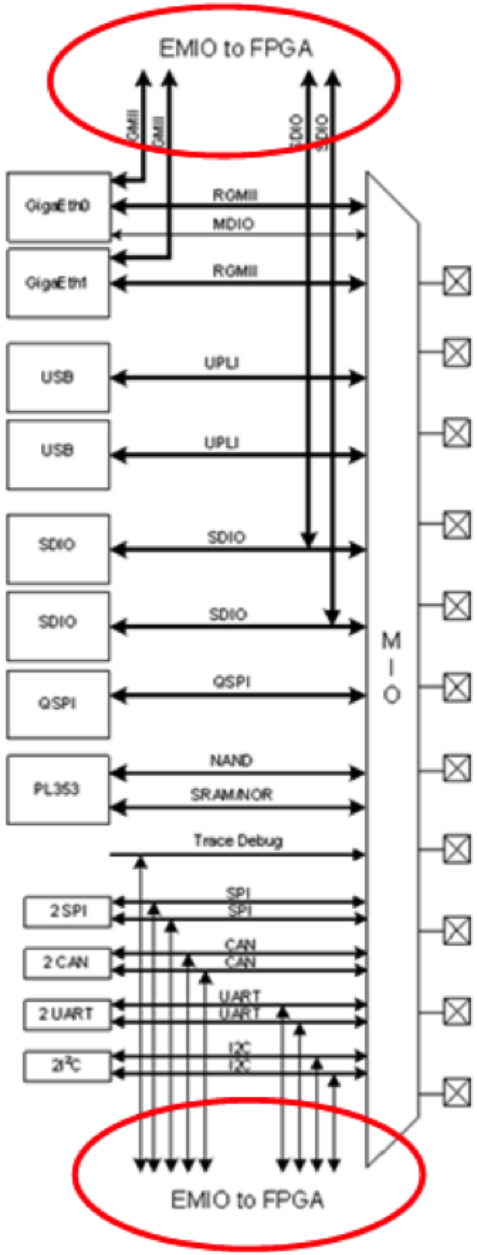
Multiplexed I/O (MIO)

- external interface to PS I/O peripheral ports
  - 54 dedicated package pins available
  - software configurable
    - automatically added to bootloader by tools
  - not available for all periphery ports
    - some ports can only use EMIO



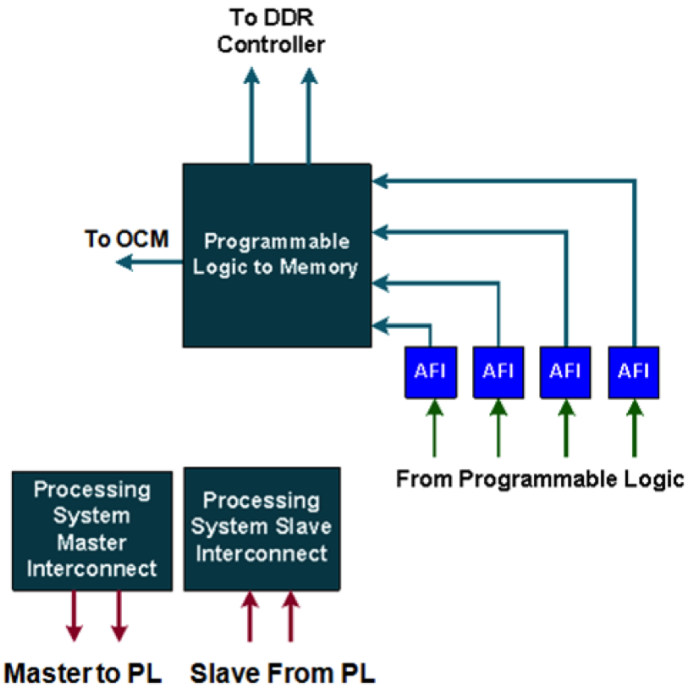
Extended Multiplexed I/O (EMIO)

- extended interface to PS I/O peripheral ports
  - EMIO: peripheral port to programmable logic
  - alternative to use MIO
  - mandatory for some peripheral ports
  - facilitates
    - connection to peripheral in programmable logic
    - use of general I/O pins to supplement MIO pin usage



PS-PL Interfaces (1)

- AXI high-performance slave ports (HP0-HP3)
  - configurable 32-bit or 64-bit data width
  - access to OCM and DDR only
  - conversion to processing system clock domain
  - AXI FIFO interface (AFI) are FIFOs (1KB) to smooth large data transfers
- AXI general-purpose ports (GP0-GP3)
  - two masters from PS to PL
  - two slaves from PL to PS
  - 32-bit data width
  - conversation and sync to processing system clock domain



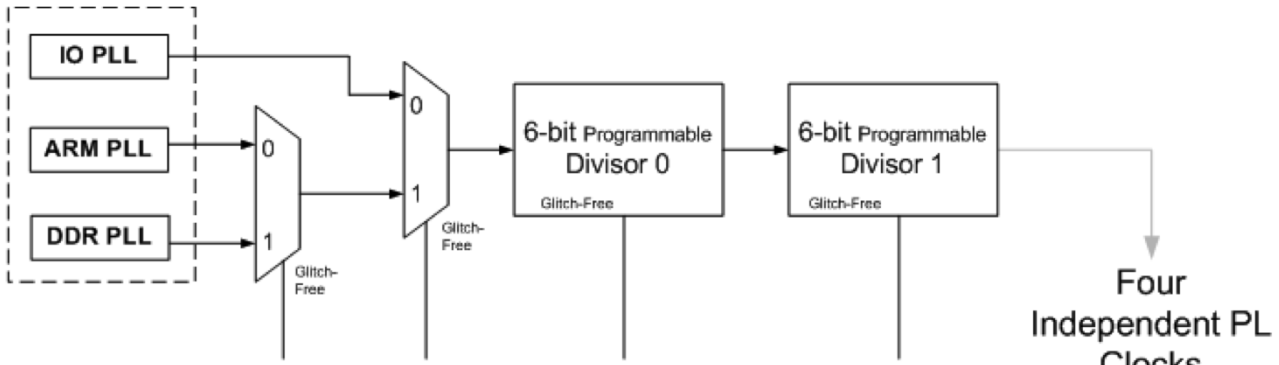
PS-PL Interfaces (2)

- one 64-bit accelerator coherence port (ACP) AXI slave interface to CPU memory
- DMA, interrupts, event signals
  - processor event bus for signaling event information to the CPU
  - PL peripheral IP interrupts to the PS general interrupt controller (GIC)
  - four DMA channel RDY/ACK signals
- extended multiplexed I/O (EMIO) allows PS peripheral ports access to PL logic and device I/O pins
- clock and resets
  - four PS clock outputs to the PL with enable control
  - four PS reset outputs to the PL
- configuration and miscellaneous

PL Clocking Sources

- PS clocks
  - PS clock source from external package pin
  - PS has three PLLs for clock generation
  - PS has four clock ports to PL
- PL has 7 series clocking resources
  - PL has a different clock source domain compared to the PS
  - the clock to PL can be sourced from the external clock capable pins
  - one of the four PS clock sources can be used for the PL
- PS architecture synchronizes the clock between PL and PS
- PL cannot supply clock source to PS
- GUI interface for PL and PS clock definition

Clocking the PL



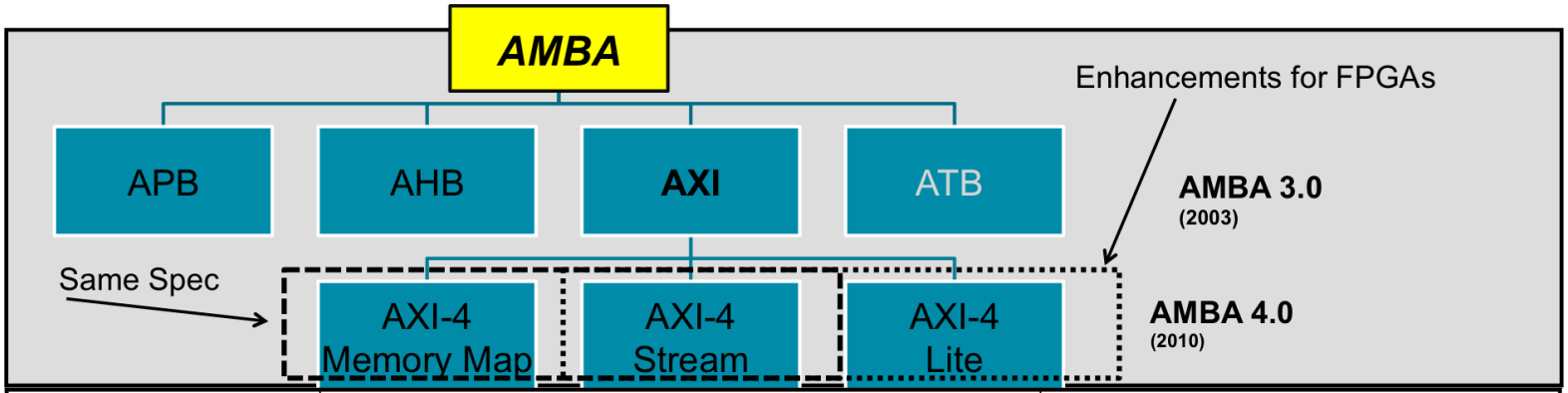
PL Fabric Clock	Control Register	Mux Ctrl Field	Mux Ctrl Field	Divider 0 Ctrl Field	Divider 1 Ctrl Field
PL Fabric 0	FPGA0_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20
PL Fabric 1	FPGA1_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20
PL Fabric 2	FPGA2_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20
PL Fabric 3	FPGA3_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20

→ FCLKCLK0
→ FCLKCLK1
→ FCLKCLK2
→ FCLKCLK3

Zynq Resets

- internal resets
  - power-on-reset (POR)
  - watchdog resets from the three watchdogs timers
  - secure violation reset
- PS resets
  - external resets: PS_SRST_B
  - warm reset: SRSTB
- PL resets
  - four reset outputs from PS to PL
  - FCLK_RESET[3:0]

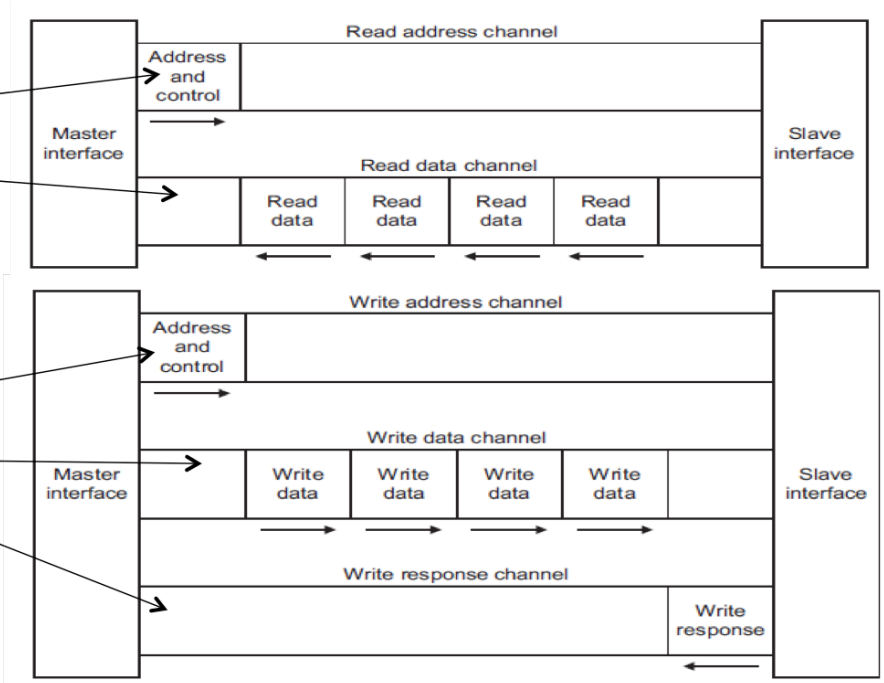
AXI is Part of ARM's AMBA Bus



Interface	Features	Similar to
Memory Map / Full (AXI4)	Traditional Address/Data Burst (single address, multiple data)	PLBv46, PCI
Streaming (AXI4-Stream)	Data-Only, Burst	Local Link / DSP Interfaces / FIFO / FSL
Lite (AXI4-Lite)	Traditional Address/Data—No Burst (single address, single data)	PLBv46-single OPB

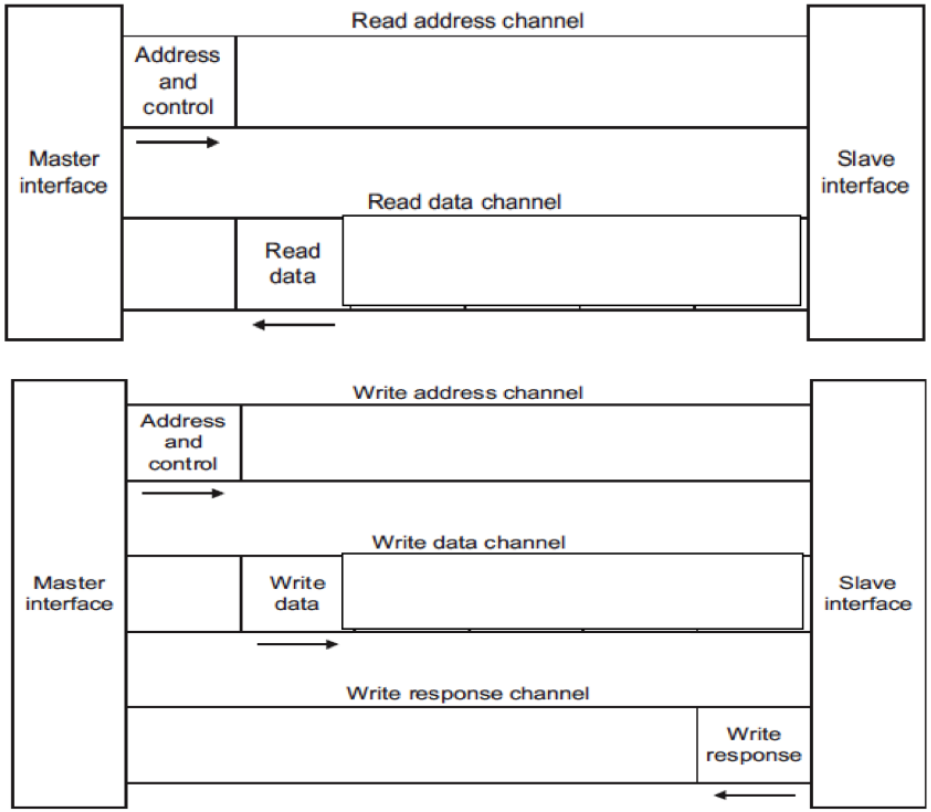
Basic AXI Signaling - 5 Channels

1. read address channel
2. read data channel
3. write address channel
4. write data channel
5. write response channel



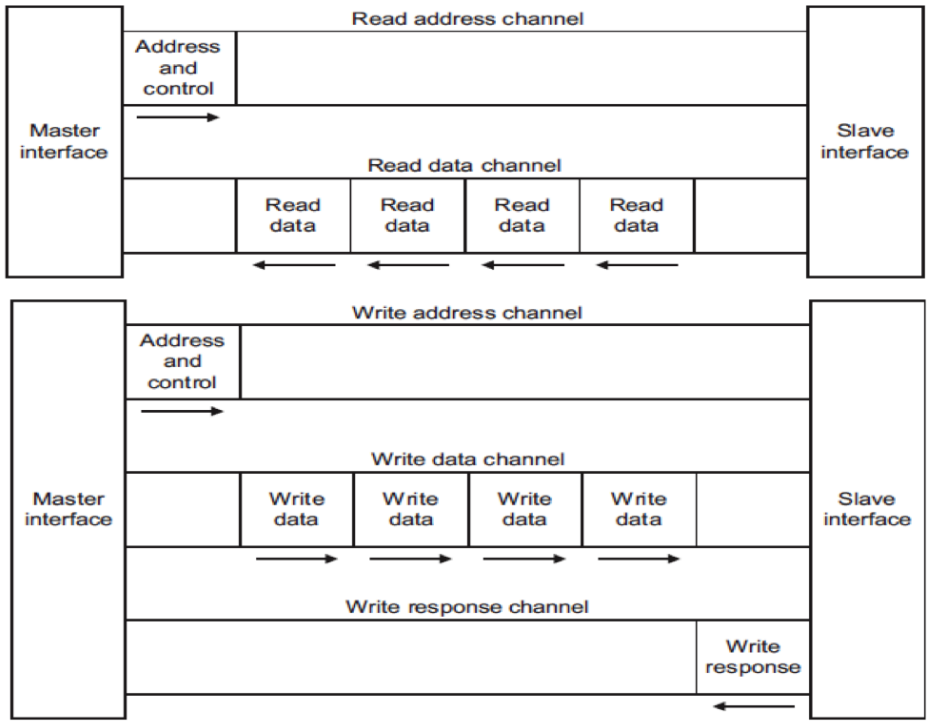
The AXI Interface - AXI4-Lite

- no burst
- data width 32 or 64
  - Xilinx IP only suppports 32-bits
- very small footprint
- bridging to AXI4 handled automatically by AXI_Interconnect



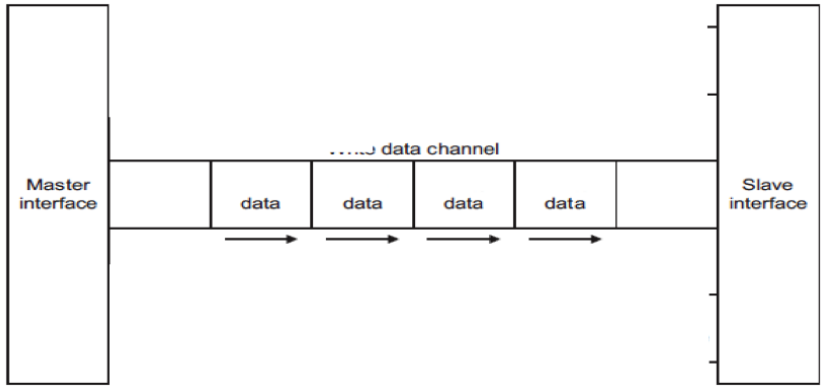
The AXI Interface - AXI4

- sometimes called "Full AXI" or "memory mapped"
  - not ARM-sanctioned names
- single address multiple data
  - burst up to 256 data beats
- data width parameterizable
  - 1024 bits



The AXI Interface - AXI4-Stream

- no address channel, no read and write, always just master to slave
  - effectively and AXI4 "write data" channel
- unlimited burst length
  - AXI4 max 256
  - AXI4-Lite does not burst
- virtually same signaling as AXI data channels
  - protocol allows merging, packing, width conversion
  - supports sparse, continuous, aligned, unaligned streams



The AXI Interface -Streaming Applications

- may not have packets
  - e.g: digital up converter:
  - no concept of address
  - free running data (in this case)
  - AXI4-stream would optimize to a very simple interface (in this case)
- may have packets
  - e.g: PCIe:
  - their packets may contain different information
  - typically bridge logic of some sort is needed

Conclusion

- the Zynq-7000 processing platform is a system-on-chip SoC processor with embedded programmable logic
- the processing system (PS) is a hard silicon dual core consisting of
  - an application processor unit
    - two ARM Cortex-A9 processors
    - NEON co-processor
    - general interrupt controller
    - general and watchdog timers
  - I/O peripherals
  - external memory interfaces
- the programmable logic (PL) consists of 7 series devices
- high performance AXI4 point-to-point interface
- tightly coupled AXI4 ports interfacing PS and PL
- PS boots from a selection of external memory devices
- PL is configured by and after PS boots
- PS provides clocking resources to PL